Optical Transceivers

FTLF8556X1YCZ

50GBASE-SR 100m 850nm Multi-Mode SFP56 Transceiver

FTLF8556x1yCz SFP56 transceivers are designed for use in single-lane, serial 4-level Pulse Amplitude Modulation (PAM4) 50GBASE-SR, as well as 2-level Amplitude Modulation 25GBASE-SR and 10GBASE-SR Ethernet links, over up to 100m OM4 Multi_x005F_xFFFE_Mode Fiber (MMF) for 50GBASE-SR and 25GBASE-SR, and up to 400m for 10GBASE_x005F_xFFFE_ SR OM4 MMF.FTLF8556x1yCz SFP56 transceivers are compatible with the applicable requirements defined in SFF-8431 (1), and compliant with the applicable requirements defined in SFF-8432 (2), IEEE 802.3cd (3), IEEE 802.3.bs (4), and RoHS compliant as described in Application Note AN-2038 (6).TheFTLF8556x1yCz SFP56 transceivers use limiting electrical interface receivers and internal re-timers, while any required Forward Error Correction (FEC) support has to reside in the host IC. Digital Diagnostics functions are available via a 2-wire serial interface, as per SFF-8472 (7).

FEATURES

- Hot-Pluggable SFP56 Footprint
- Duplex LC connector
- Tri-Rate, Dual-Rate and Single-Rate Options
- Power Dissipation < 1.5W
- 0°C to 70°C Commercial Temperature Range
- Single 3.3Vpower supply
- Maximum Link Length of 100m OM4 MMF
- 850nm VCSEL Laser
- Limiting Electrical Interface Receiver
- Internal Re-timer
- Built-in Digital Diagnostic Functions
- Bail and Pull tab options
- RoHS Compliant

APPLICATIONS

- 50GBASE-SR
- 25GBASE-SR
- 10GBASE-SR

COHERENT

Product Selection

FTLF8556x1yCz

Part Number	Data Rate Supported		
	50GBASE-SR	25GBASE-SR	10GBASE-SR
FTLF8556E1yCL	✔	X	X
FTLF8556D1yCV	✔	✔	✔
FTLF8556D1yCW	✔	✔	✔

I. Pin Descriptions

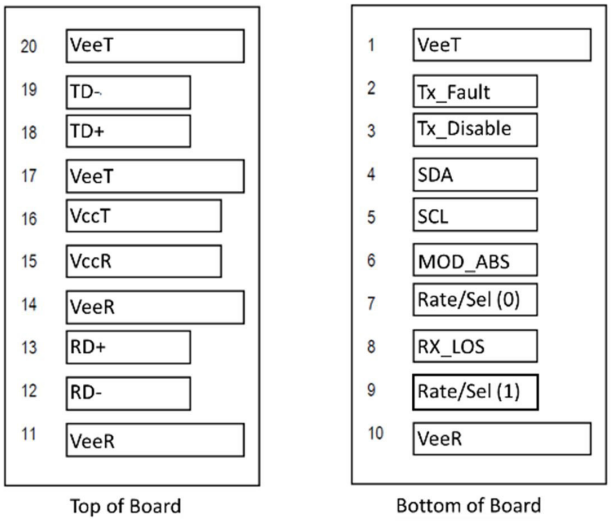


Fig.1a. Diagram of SFP+ transceiver electrical pad pin numbers and names

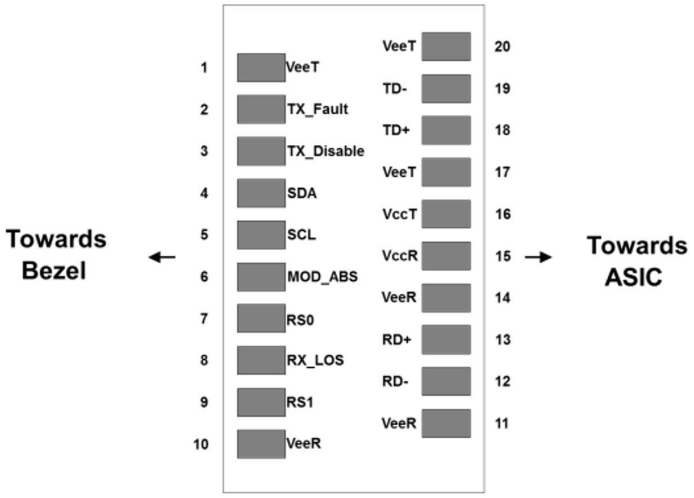


Fig.1b. Diagram of Host Board Connector Block Pin Numbers and

Pin	Symbol	Name/Description	Notes
1	V_{EET}	Transmitter Ground (Common with Receiver Ground)	1
2	T_{FAULT}	Transmitter Fault.	2,3
3	T_{DIS}	Transmitter Disable. Laser output disabled on high or open.	4
4	SDA	2-wire Serial Interface Data Line	2
5	SCL	2-wire Serial Interface Clock Line	2
6	MOD_ABS	Module Absent. Grounded within the module	5
7	RS0	Rate Select 0. See Sec. X.	5
8	RX_LOS	Loss of Signal indication. Logic 0 indicates normal operation.	6
9	RS1	Rate Select 1. See Sec. X.	5
10	V_{EER}	Receiver Ground (Common with Transmitter Ground)	1
11	V_{EER}	Receiver Ground (Common with Transmitter Ground)	1
12	RD-	Receiver Inverted DATA out. AC Coupled	
13	RD+	Receiver Non-inverted DATA out. AC Coupled	
14	V_{EER}	Receiver Ground (Common with Transmitter Ground)	1
15	V_{CCR}	Receiver Power Supply	7
16	V_{CCT}	Transmitter Power Supply	7
17	V_{EET}	Transmitter Ground (Common with Receiver Ground)	1
18	TD+	Transmitter Non-Inverted DATA in. AC Coupled.	
19	TD-	Transmitter Inverted DATA in. AC Coupled.	
20	V_{EET}	Transmitter Ground (Common with Receiver Ground)	1

Notes
1. Circuit ground is internally isolated from chassis ground.
2. Open collector/drain output, which should be pulled up with a 4.7k to 10k Ohm resistor on the host board if intended for use. Pull up voltage should be between 2.0V to Vcc + 0.3V.
3. A high output indicates a transmitter fault caused by either the TX bias current or the TX output power exceeding the preset alarm thresholds. A low output indicates normal operation. In the low state, the output is pulled to <0.8V.
4. Laser output disabled on T_{DIS} >2.0V or open, enabled on T_{DIS} <0.8V.
5. Internally pulled down per SFF-8431 Rev 4.1.
6. LOS is open collector output. Should be pulled up with 4.7k to 10kΩ on host board to a voltage between 2.0V and Vcc + 0.3V. Logic 0 indicates normal operation; logic 1 indicates loss of signal.
7. Internally connected.

II. Absolute Maximum Ratings

Exceeding the limits below may damage the transceiver module permanently.

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Maximum Supply Voltage	Vcc	-0.5		4.0	V	
Storage Temperature	T_S	-40		85	°C	
Case Operating Temperature	T_A	0		70	°C	
Relative Humidity	RH	0		85	%	1
Receiver Damage Threshold				5	dBm	

Notes:
1. Non-condensing.

III. Electrical Characteristics (T_{OP} = 0 to 70 °C, V_{CC} = 3.14 to 3.46 Volts)

The electrical interface of Finisar® FTLF8556x1yCz SFP56 transceivers is compliant to the applicable requirements defined in CEI-56G-VSR.

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Supply Voltage	Vcc	3.14		3.46	V	
Supply Current	Icc			478	mA	
Transmitter						
Input differential impedance	R_{in}		100		Ω	1
Single-ended data input swing	Vin,pp	180		900	mV	
Transmit Disable Voltage	V_D	2		Vcc	V	
Transmit Enable Voltage	V_{EN}	Vee		Vee+ 0.8	V	
Receiver						
Differential data output swing	Vout,pp	185		425	mV	2, 3
Data output rise time, fall time	t_r	9.5			ps	4
LOS Fault	$V_{LOS\ fault}$	2		Vcc_{HOST}	V	5
LOS Normal	$V_{LOS\ norm}$	Vee		Vee+0.8	V	5
Power Supply Noise Tolerance	VccT/VccR	Per SFF-8431 Rev 4.1			mVpp	

Notes:
1. Connected directly to TX data input pins. AC coupling from pins into laser driver IC.
2. Into 100Ω differential termination.
3. Limiting electrical interface
4. 50GBASE-R: 20 – 80 %. Measured with Module Compliance Test Board and OMA test pattern. Use of four 1's and four 0's in sequence in the PRBS^9 is an acceptable alternative [1].
5. LOS is an open collector output. Should be pulled up with 4.7kΩ – 10kΩ on the host board. Normal operation is logic 0; loss of signal is logic 1. Maximum pull-up voltage is 5.5V .

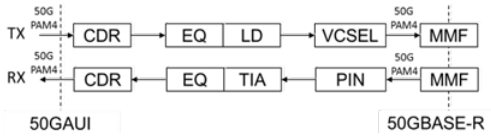


Figure 2. Duplex 50G Transceiver Architecture

The FTLF8556x1yCz allows the host to select pre-set levels of optimization of the receiver's electrical high-speed output signals, via the 2-wire communication (as defined in the SFF-8472[2]), while it provides adaptive Continuous Time Linear Equalization (CTLE) on its transmitter electrical high-speed inputs.

IV. Optical Characteristics (T_{OP} = 0 to 70 °C, V_{CC3} = 3.14 to 3.46 Volts)

50GBASE-SR Specifications

The optical interface of Finisar® FTLF8556x1yCz SFP56 transceivers is compliant to the applicable requirements defined in IEEE 802.3cd (3), Tab. 138–8 and 138-9:

Parameter		Symbol	Min	Typ	Max	Unit	Ref.
Transmitter							
Signaling Rate				26.5625		GBd	
Center Wavelength		λ	840		860	nm	
RMS Spectral Width		ΣΩ			0.6	Nm	
Average Launch Power			-6.5		4	dBm	
Outer Optical Modulation Amplitude (OMA)		TX_{OMA_outer}	-4.5		3	dBm	1
Transmitter and Dispersion Eye Closure		TDECQ			4.5	dB	
Launch Power in OMA_{outer} minus TDECQ			-5.9			dBm	
Average Launch power of OFF transmitter		POFF			-30	dBm	
Extinction Ratio		ER	3			dB	
$RIN_{12}OMA$			-128			dB/Hz	
Optical Return Loss Tolerance					12	dB	
Transmitter Reflectance					-26	dB	2
Encircled flux	at 19µm		86%				3
	at 4.5µm				30%		
Receiver							
Center Wavelength			840		860	nm	
Average Receive power			-8.4		4	dBm	4
Receive Power, in OMA					3	dBm	
Receiver Sensitivity, in OMA, at BER 2.4 $x10^{-4}$		RS			Equation (138–1)	dBm	5
Stressed Receiver Sensitivity, in OMA, at BER 2.4 $x10^{-4}$		$SRS_{—OMAouter}$			-3.4	dBm	6
Receiver Reflectance					-12	dB	
LOS Deassert		LOSD			-13	dBm	
LOS Assert		LOSA	-30			dBm	
LOS Hysteresis		HYS	0.5			dB	
Conditions of stressed receiver sensitivity test							7
Stressed Eye Closure		SECQ		4.5		dB	

Notes:
1. Even if the TDECQ < 1.4 dB, the TX_{OMA_outer} (min) must exceed this value.
2. Transmitter reflectance is defined looking into the transmitter.
3. If measured into type A1a.2 or type A1a.3, or A1a.4, 50 µm fiber, in accordance with IEC 61280-1-4.
4. Average receive power is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ up to 4.5 dB. RS = max (-6.5, SECQ – 7.9) (dB)
6. Measured with conformance test signal at TP3 (see 138.8.10) for the BER specified in 138.1.1.
7. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

25GBASE-SR Specifications (only applicable to FTLF8556D1yCW and FTLF8556D1yCV)

The optical interface of Finisar® FTLF8556D1yCz SFP56 transceivers at 25Gb/s is compliant to the applicable requirements defined in IEEE 802.3by, Sec 112.6.1 and 112.6.2.

Parameter		Symbol	Min	Typ	Max	Unit	Ref.
Transmitter							
Signaling Rate				25.78125		Gb/s	
Center Wavelength		λ	840		860	nm	
RMS Spectral Width		SW			0.6	Nm	
Average Launch Power			-8.4		2.4	dBm	
Outer Optical Modulation Amplitude (OMA)		OMA	-6.4		3	dBm	1
Transmitter and Dispersion Eye Closure		TDEC			4.3	dB	
Launch Power in OMA minus TDEC			-7.3			dBm	
Average Launch power of OFF transmitter		P_{OFF}			-30	dBm	
Extinction Ratio		ER	2			dB	
Optical Return Loss Tolerance					12	dB	2
Transmitter Reflectance					-26	dB	2
Encircled flux	at 19µm		86%				3
	at 4.5µm				30%		
Receiver							
Center Wavelength			840		860	nm	
Average Receive power			-10.3		2.4	dBm	4
Receive Power, in OMA					3	dBm	
Stressed Receiver Sensitivity, in OMA, at BER 5 x10^{-5}		SRS			-5.2	dBm	5
Receiver Reflectance					-12	dB	
LOS Deassert		LOSD			-13	dBm	
LOS Assert		LOSA	-30			dBm	
LOS Hysteresis		HYS	0.5			dB	
Conditions of stressed receiver sensitivity test							7
Stressed Eye Closure		SEC		4.5		dB	
Stressed Eye J2 Jitter			0.39		UI		
Stressed Eye J4 Jitter				0.53	UI		
OMA			3		dBm		
Stressed receiver eye mask definition {X1, X2, X3, Y1, Y2, Y3} Hit ratio 5 × 10^{-5} hits per sample			{0.28, 0.5, 0.5, 0.33, 0.33, 0.4}				

Notes:
1. Even if the TDEC < 0.9 dB, the OMA (min) must exceed this value.
2. Transmitter reflectance is defined looking into the transmitter.
3. If measured into type A1a.2 or type A1a.3, or A1a.4, 50 µm fiber, in accordance with IEC 61280-1-4.
4. Average receive power is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Measured with conformance test signal at TP3 (see 95.8.8) for the BER specified in 95.1.1.
6. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

10GBASE-SR Specifications (only applicable to FTLF8556D1yCW)

Parameter		Symbol	Min	Typ	Max	Unit	Ref.
Transmitter							
Signaling Rate				10.3125		Gb/s	
Center Wavelength		λ	840		860	nm	
RMS Spectral Width		SW			0.45	Nm	
Average Launch Power			-7.3		1.5	dBm	
Optical Modulation Amplitude (OMA)		OMA	-4.3			dBm	
Average Launch power of OFF transmitter		P_{OFF}			-30	dBm	
Extinction Ratio		ER	3			dB	
Optical Return Loss Tolerance					12	dB	
Transmitter Reflectance					-26	dB	1
Encircled flux	at 19µm		86%				2
	at 4.5µm				30%		
Receiver							
Center Wavelength			840		860	nm	
Average Receive Power			-9.9		+1.5	dBm	
Receive Power, in OMA					-11.1	dBm	3
Stressed Receiver Sensitivity, in OMA		SRS			-7.5	dBm	4
Receiver Reflectance					-12	dB	
LOS Deassert		LOSD			-13	dBm	
LOS Assert		LOSA	-30			dBm	
LOS Hysteresis		HYS	0.5			dB	

Notes:
1. Transmitter reflectance is defined looking into the transmitter.
2. If measured into type A1a.2 or type A1a.3, or A1a.4, 50 µm fiber, in accordance with IEC 61280-1-4.
3. Measured with worst ER, BER < 10-12, PRBS 231-1
4. Per IEEE 802.3-2012

V. General Specifications

Rate	Nominal Rate	Symbol	Min	Fiber Type	Core Size	Modal Band-width	Link Length
		Optical	max BER	(850nm MMF)	(um)	(MHZ x km)	(max)
10G	10.3125 NRZ	10GBASE-SR	1.0E-12	FDDI	62.5	160	26m
				OM1	62.5	200	33m
				-	50	400	66m
				OM2	50	500	82m
				OM3	50	2000	300m
				OM4	50	4700	400m
25G	25.78125 NRZ	25GBASE-SR	5.0E-05	OM3	50	2000	70m
				OM4	50	4700	100m
50G	26.5625 PAM4	50GBASE-SR	2.4E-04	OM3	50	2000	70m
				OM4 & OM5	50	4700	100m

VII. Environmental Specifications

Finisar® FTLF8556x1yCz SFP56 transceivers have an operating case temperature range from 0°C to +70°C.

Environmental Specifications	Symbol	Min	Typ	Max	Units	Ref.
Operating Case Temperature	T_{op}	0		70	°C	
Storage Temperature	T_{sto}	-40		85	°C	

VII. Regulatory Compliance

Finisar® FTLF8556x1yCz SFP56 transceivers are RoHS compliant. Copies of certificates are available from II-VI Incorporated upon request.

Finisar® FTLF8556x1yCz SFP56 transceiver modules are Class 1 laser eye safety compliant per IEC 60825-1.

CAUTION: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

VIII. Digital Diagnostic Functions

Finisar® FTLF8556x1yCz SFP56 transceivers support the 2-wire serial communication protocol as defined in the SFF-8472. It is very closely related to the E²PROM defined in the GBIC standard, with the same electrical specifications.
The standard SFP56 serial ID provides access to identification information that describes the transceiver's capabilities, standard interfaces, manufacturer, and other information.
Additionally, Finisar® SFP56 transceivers provide an enhanced digital diagnostic monitoring interface, which allows real-time access to device operating parameters such as transceiver temperature, laser bias current, transmitted optical power, received optical power and transceiver supply voltage. It also defines a sophisticated system of alarm and warning flags, which alerts end-users when particular operating parameters are outside of a factory set normal range.
SFF-8472 defines a 256-byte memory map in E²PROM that is accessible over a 2-wire serial interface at the 8-bit address 1010000X (A0h). The digital diagnostic monitoring interface makes use of the 8-bit address 1010001X (A2h), so the originally defined serial ID memory map remains unchanged. The interface is identical to, and is thus fully backward compatible with both the GBIC Specification and the SFP Multi Source Agreement. The complete interface is described in Finisar Application Note AN-2030 [7].
The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through a 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL, Mod Def 1) is generated by the host. The positive edge clocks data into the SFP transceiver into those segments of the E²PROM that are not write-protected. The negative edge clocks data from the SFP transceiver. The serial data signal (SDA, Mod Def 2) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially.

For more information, please refer to (7) (8).

IX. Digital Diagnostic Specifications

FTLF8536P5xyz transceivers can be used in host systems that require either internally or externally calibrated digital diagnostics.

Parameter	Value	Units	Accuracy
Operating Range for rated accuracy			
Internally measured transceiver temperature (range)	0 to 70	ºC	±5ºC
Internally measured transceiver supply voltage (range)	3.14 to 3.46	V	±0.1V
Measured TX bias curren[t(1)] (range)	0 to 20	mA	±10%
Measured TX output power (range)	-6 to 4	dBm	±3dB
Measured RX received average optical power (range)	-7.9 to 4	dBm	±2dB
Max Reporting Range			
Internally measured transceiver temperature	-5 to 75	ºC	-
Internally measured transceiver supply voltage	2.8 to 4.0	V	-
Measured TX bias current	0 to 20	mA	-
Measured TX output power	-9 to 7	dBm	-
Measured RX received average optical power	-10 to 6	dBm	-

Notes:
1. Accuracy of measured Tx bias current is 10% of the actual bias current from the laser driver to the laser.

The FTLF8556x1yCz will update the EEPROM bytes containing the alarm and warning thresholds of the transmitter's and receiver's optical power according to the rate selected by the host. The checksum in byte 95dec of address A2h will be updated accordingly.

X. Rate Select Logic Table

The FTLF8556D1yCW is a tri-rate transceiver, and the host can set the transceiver's rate-select bits or pins to set the transceiver internal re-timer for 50GBASE-R, 25GBASE- R or 10GBASE-R operation, as shown in the following table.

RS0 Logic OR of pin 7 and bit 110.3 (A2h)	RS1 Logic OR of pin 9 and bit 118.3 (A2h)	Transceiver's Re-timer Operation
0	0	10GBASE-R
0	1	25GBASE-R
1	0	Disregarded (i.e. keeps current rate)
1	1	50GBASE-R

The default status at the transceiver's power-up is 10GBASE-R, and its bits 110.3 and 118.3 (A2h) are set to 0 by default.
The sequence used to change the rate-select pins/bits (RS0/RS1) is important. For instance, changing from 50GBASE-R (1/1) to 10GBASE-R (0/0) can set the internal re- timer through two different operating rate sequences:
- 1/1 (50GBASE-R) → 1/0 (keeps 50GBASE-R) → 0/0 (10GBASE-R).
- 1/1 (50GBASE-R) → 0/1 (25GBASE-R) → 0/0 (10GBASE-R).

The FTLF8556D1yCV is a dual-rate transceiver, and the host can set the transceiver's rate-select bits and/or pins to set the transceiver internal re-timer for 50GBASE-SR or 25GBASE-SR operation, as shown in the following table.

Logic OR of pin 7 and bit 110.3 (A2h)	Transceiver's Re-timer Operation
0	25GBASE-SR
1	50GBASE-SR

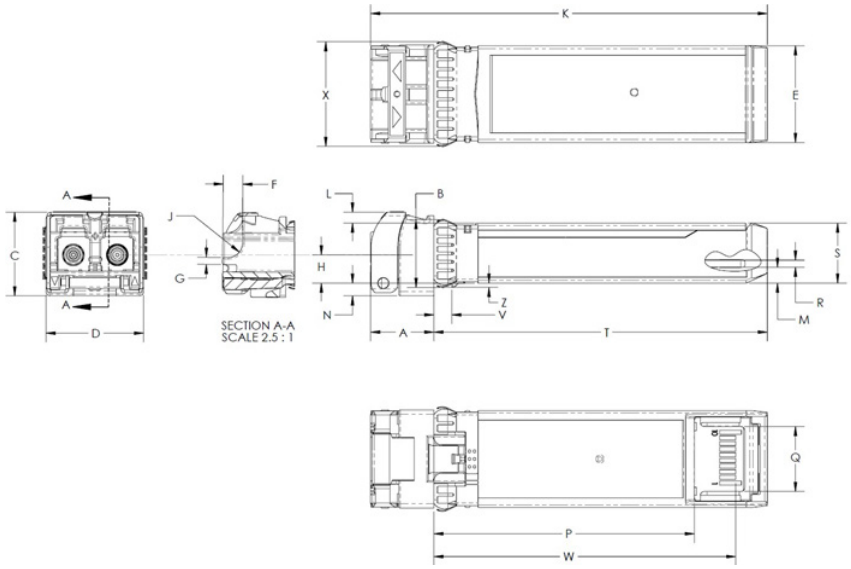
The transceiver will disregard the status of the pin 9 and of the bit 118.3 (A2h).
The default status at the transceiver's power-up is 10GBASE-SR, and its bit 110.3 (A2h) is set to 0 by default.

XI. SFF-8431 Power-up Sequence

FTLF8556x1yCz's power consumption may exceed the limit of 1W specified for Power Level I transceivers [1], for which a power-up sequence is recommended. However, the FTLF8556x1yCz is factory set to power-up directly to its operating conditions. Upon request, it can be factory set to follow the power-up sequence, as per [1]. In power level I, the FTLF8556x1yCz does not carry traffic, but its 2-wire serial communication is active. Please refer to [1] and Finisar Application Note AN-2076 for additional details.

XII. Mechanical Specifications

Finisar FTLF8556x1yCz SFP56 transceivers are compatible with the SFF-8432 specification for improved pluggable form factor, and shown here for reference purposes only. Bail and pull tab color is black.



ITEM	DIM (mm)	TOL (mm)
A	9.00	± 0.3
B	9.60	± 0.5
C	11.90	REF
D	13.85	± 0.15
E	13.70	± 0.1
F	2.80	± 0.2
G	1.00	± 0.2
H	4.00	REF
J	2.00	± 0.2
K	56.50	REF
L	1.60	± 0.5
M	2.25	± 0.1
N	1.80	± 0.1
P	37.10	± 0.3
Q	9.15	± 0.15
R	1.00	± 0.1
S	8.55	± 0.15
T	47.50	± 0.2
V	2.55	± 0.1
W	43.00	± 0.2
X	14.70	± 0.5
Z	0.55	± 0.15

Figure 3. FTLF8556x1BCz (Bail latch) Mechanical Dimensions and Tolerances

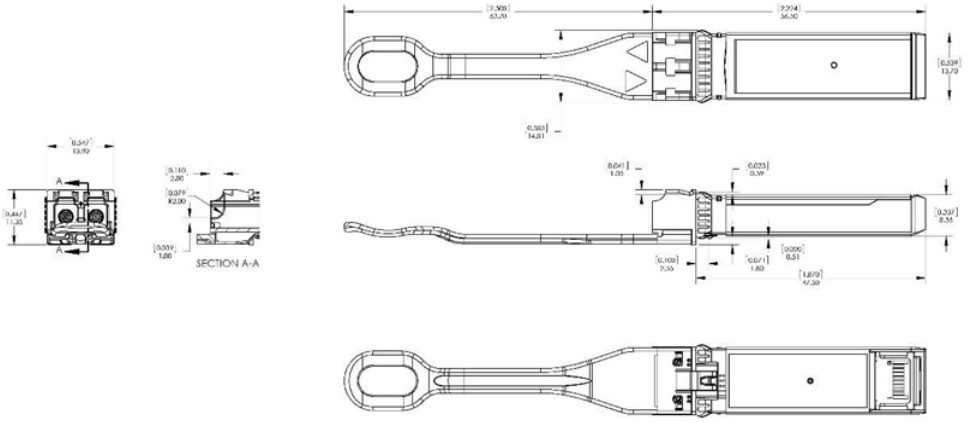
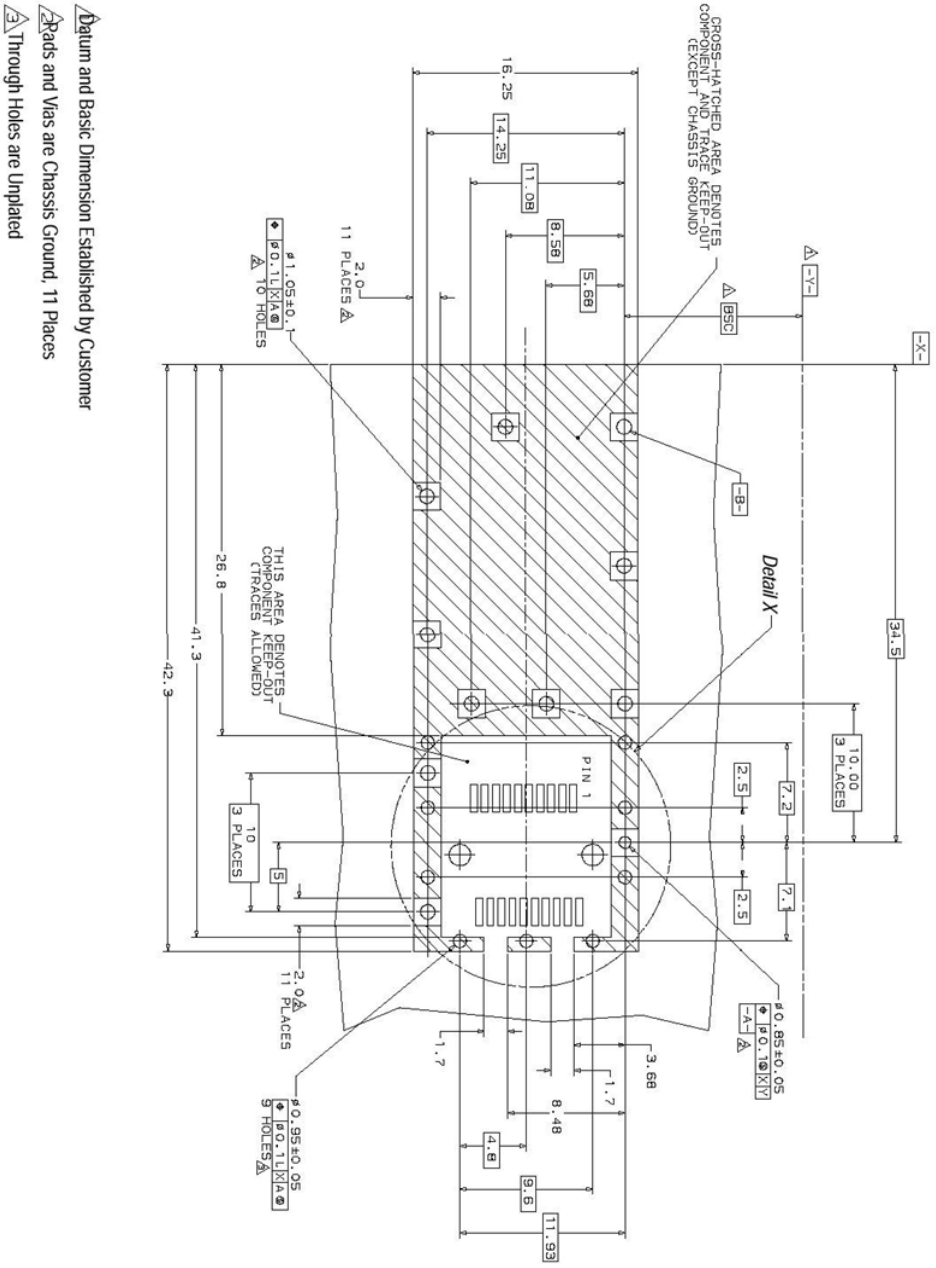
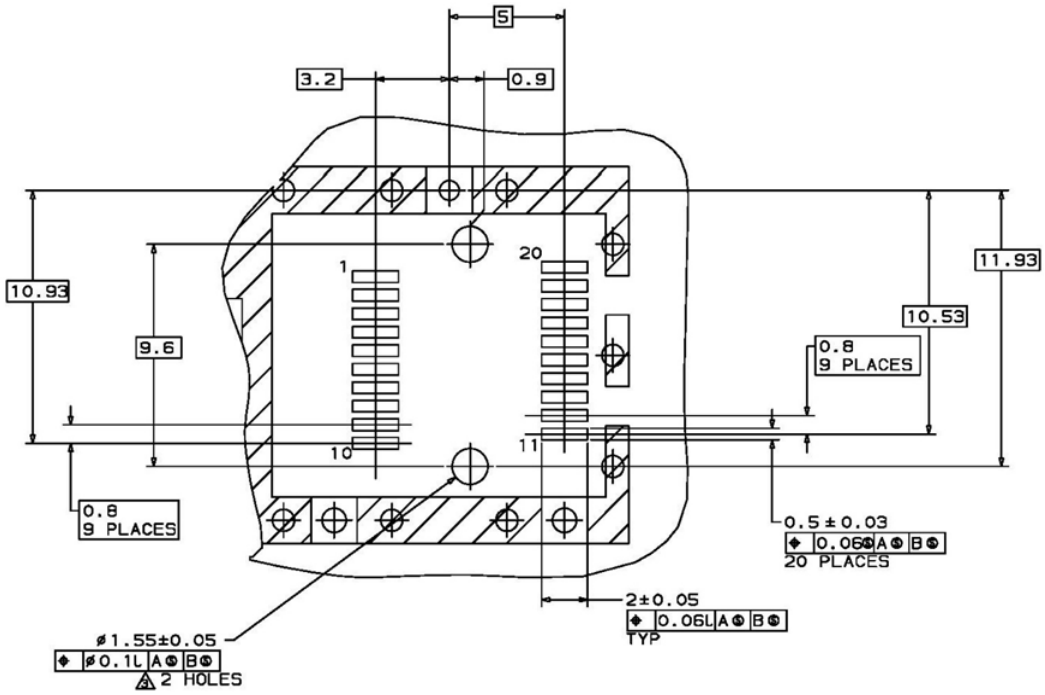
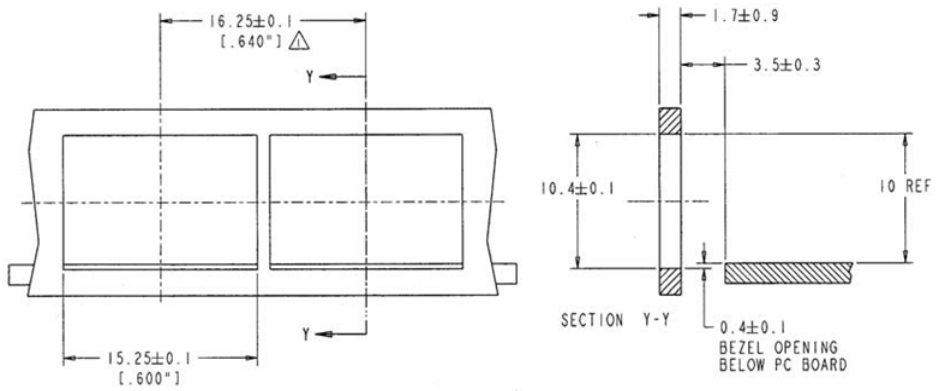


Figure 4. FTLF8556x1PCz (Pull tab) Mechanical Dimensions and Tolerances

XIII. PCB Layout and Bezel Recommendations







NOTES:

1. MINIMUM PITCH ILLUSTRATED, ENGLISH DIMENSIONS ARE FOR REFERENCE ONLY
2. NOT RECOMMENDED FOR PCI EXPANSION CARD APPLICATIONS

XIV. Host - Transceiver Interface Block Diagram

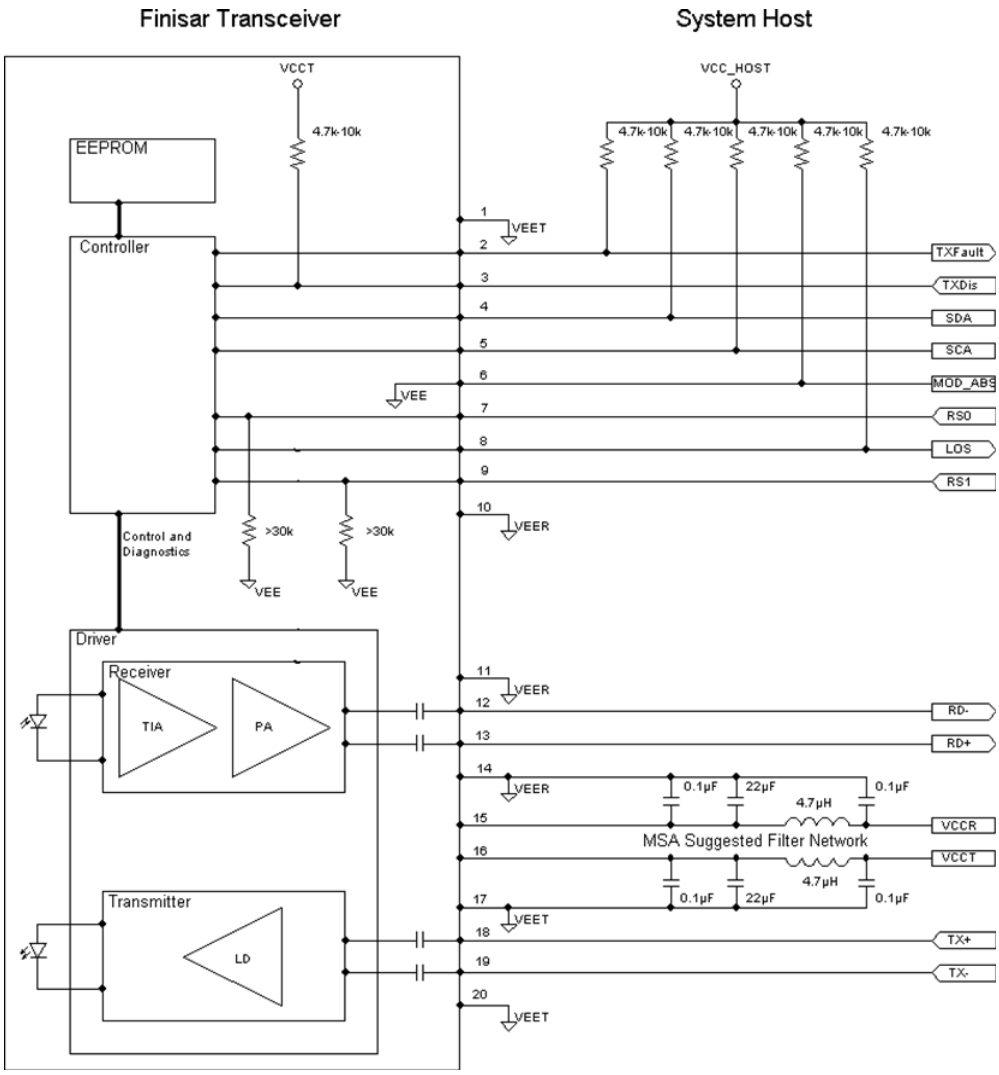


Figure 7. Host-Module Interface

XV. References

1. “Specifications for Enhanced 8.5 and 10 Gigabit Small Form Factor Pluggable Module ‘SFP+’”, SFF Document Number SFF-8431, Revision 4.1. 1

2. “Improved Pluggable Formfactor”, SFF Document Number SFF-8432, Revision 5.0.

3. IEEE Std 802.3cd, Clause 138, PMD Type 50GBASE-SR. IEEE Standards Department. “50GBASE-SR: IEEE 802.3 Physical Layer specification for 50Gb/s using 50GBASE-R encoding over a multimode fiber. (See IEEE Std 802.3, Clause 138)”.

4. IEEE 802.3bs / CDAUI-8.

5. Directive 2011/65/EU of the European Council Parliament and of the Council, “on the restriction of the use of certain hazardous substances in electrical and electronic equipment”, as well as Commission Delegated Directive (EU) 2015/863 amending Annex II to Directive 2011/65/EU. Certain products may use one or more exemptions as allowed by the Directive..

6. “Application Note AN-2038: “II-VI Implementation of RoHS Compliant Transceivers”.

7. “Digital Diagnostics Monitoring Interface for Optical Transceivers”. SFF Document Number SFF-8472, Revision 12.4.

8. Application Note AN-2030: “Digital Diagnostics Monitoring Interface for SFP Optical Transceivers”.

XVI. Ordering Information

Part Number	Unlocking Mechanism	Data Rate
FTLF8556E1BCL	Bail latch	50GbE only
FTLF8556D1BCV	Bail latch	50GbE and 25GbE
FTLF8556D1BCW	Bail latch	50GbE, 25GbE and 10GbE
FTLF8556E1PCL	Pull tab	50GbE only
FTLF8556D1PCV	Pull tab	50GbE and 25GbE
FTLF8556D1PCW	Pull tab	50GbE, 25GbE and 10GbE

1 The FTLF8556x1yCz SFP56 transceiver is not compliant with below timing specs defined in SFF-8431, Rev 4.1:

Parameter	Symbol	SFF-8431 Rev 4.1 Spec	FTLF8556x1yCz Spec
Time to initialize 2- wire interface	t_2w_start_up	300 ms Max	1000 ms Max
Time to initialize	t_start_up	300 ms Max	2500 ms Max (including CDR locking time)
RS0, RS1 rate select timing non FC	t_RS0, t_RS1	24 ms Max	1800 ms Max

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