Product Specification

8 Gigabit RoHS Compliant Long-Wavelength SFP+ Transceiver

FTLF1428P3BNV

PRODUCT FEATURES

- Up to 8.5 Gb/s bi-directional data links
- Hot-pluggable SFP+ footprint
- Built-in digital diagnostic functions
- 1310nm DFB laser transmitter
- Duplex LC connector
- RoHS compliant and Lead Free
- Up to 10 km on 9/125µm SMF
- Metal enclosure, for lower EMI
- Single 3.3V power supply
- Extended operating temperature range: -5°C to 85°C

APPLICATIONS

- Tri Rate 2.125 / 4.25 / 8.5 Gb/s Fibre Channel through Rate Select

Finisar's FTLF1428P3BNV SFP+ transceivers are designed for use in Fibre Channel links up to 8.5 Gb/s data rate and up to 10 km link length. They are compliant with FC-PI-4 Rev. 8.00[1] and SFF-8472 Rev 10.3[3], and compatible with SFF-8432[2] and applicable portions of SFF-8431 Rev. 3.0[4]. The optical transceiver is compliant per the RoHS Directive 2011/65/EU[5]. See Finisar Application Note AN-2038 for more details[6].

PRODUCT SELECTION

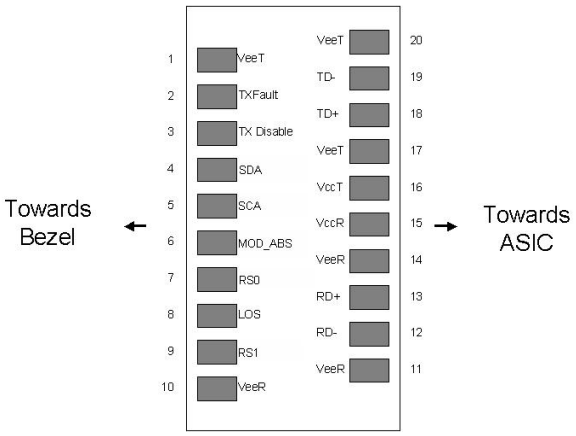
FTLF1428P3BNV

I. Pin Descriptions

Pin	Symbol	Name/Description	Ref.
1	V_{EET}	Transmitter Ground (Common with Receiver Ground)	1
2	T_{FAULT}	Transmitter Fault.	2
3	T_{DIS}	Transmitter Disable. Laser output disabled on high or open.	3
4	SDA	2-wire Serial Interface Data Line (MOD-DEF2)	4
5	SCA	2-wire Serial Interface Clock (MOD-DEF1)	4
6	MOD_ABS	Module Absent, connected to V_{EET} or V_{EER}	4
7	RS0	Rx Rate Select: Open or Low = 2.125 or 4.25 Gb/s Fibre Channel (Low Bandwidth) High = 8.5 Gb/s Fibre Channel (High Bandwidth)	5
8	LOS	Loss of Signal indication. Logic 0 indicates normal operation.	6
9	RS1	Tx Rate Select: Open or Low = 2.125 or 4.25 Gb/s Fibre Channel (Low Bandwidth) High = 8.5 Gb/s Fibre Channel (High Bandwidth)	5
10	V_{EER}	Receiver Ground (Common with Transmitter Ground)	1
11	V_{EER}	Receiver Ground (Common with Transmitter Ground)	1
12	RD-	Receiver Inverted DATA out. AC Coupled	
13	RD+	Receiver Non-inverted DATA out. AC Coupled	
14	V_{EER}	Receiver Ground (Common with Transmitter Ground)	1
15	V_{CCR}	Receiver Power Supply	
16	V_{CCT}	Transmitter Power Supply	
17	V_{EET}	Transmitter Ground (Common with Receiver Ground)	1
18	TD+	Transmitter Non-Inverted DATA in. AC Coupled.	
19	TD-	Transmitter Inverted DATA in. AC Coupled.	
20	V_{EET}	Transmitter Ground (Common with Receiver Ground)	1

Notes:

1. Circuit ground is internally isolated from chassis ground.
2. T_{FAULT} is an open collector/drain output, which should be pulled up with a 4.7k – 10k Ohms resistor on the host board if intended for use. Pull up voltage should be between 2.0V to Vcc + 0.3V. A high output indicates a transmitter fault caused by either the TX bias current or the TX output power exceeding the preset alarm thresholds. A low output indicates normal operation. In the low state, the output is pulled to <0.8V.
   - T_{FAULT} is latched
   - Tx_Fault occurs under the condition of logical OR of Tx Power High Alarm and Tx Bias High Alarm
   - When Tx_Fault occurs, laser safety function is activated and laser is shut down. The Tx Power High Alarm/Warning bits and Tx Bias High Alarm/Warning bits are cleared during the laser shut down. The Tx Power Low Alarm/Warning bits and Tx Bias Low Alarm/Warning bits are set during the laser shut down.
3. Laser output disabled on T_{DIS} >2.0V or open, enabled on T_{DIS} <0.8V.
4. Should be pulled up with 4.7k – 10kohms on host board to a voltage between 2.0V and 3.6V. MOD_ABS pulls line low to indicate module is plugged in.
5. Rate select can also be set through the 2-wire bus in accordance with SFF-8472 v. 10.2. Rx Rate Select is set at Bit 3, Byte 110, Address A2h. Tx Rate Select is set at Bit 3, Byte 118, Address A2h. Note: writing a "1" selects maximum bandwidth operation. Rate select is the logic OR of the input state of Rate Select Pin and 2-wire bus.
6. LOS is open collector output. Should be pulled up with 4.7k – 10kohms on host board to a voltage between 2.0V and 3.6V. Logic 0 indicates normal operation; logic 1 indicates loss of signal.



Pinout of Connector Block on Host Board

II. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Maximum Supply Voltage	Vcc	-0.5		4.5	V	
Storage Temperature	T_S	-40		85	°C	
Case Operating Temperature	T_{OP}	-5		85	°C	
Relative Humidity	RH	0		85	%	1

III. Electrical Characteristics (T_{OP} = -5 to 85 °C, V_{CC} = 3.00 to 3.60 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Supply Voltage	Vcc	3.00		3.60	V	2
Supply Current	Icc		200	300	mA	2
Transmitter						
Input differential impedance	R_{in}		100		Ω	3
Single ended data input swing	Vin,pp	90		1000	mV	
Transmit Disable Voltage	V_D	2		Vcc	V	
Transmit Enable Voltage	V_{EN}	Vee		Vee+ 0.8	V	4
Receiver						
Single ended data output swing	Vout,pp	185		425	mV	5
Data output rise/fall time, 2.125, 4.25 Gb/s	t_r, t_f			120	ps	6
Data output rise/fall time, 8.5 Gb/s	t_r, t_f			60	ps	6
LOS Fault	$V_{LOS\ fault}$	2		Vcc_{HOST}	V	7
LOS Normal	$V_{LOS\ norm}$	Vee		Vee+0.8	V	7
Power Supply Rejection	PSR	100			mVpp	8
Deterministic Jitter Contribution < 4.25 Gb/s	RX Δ DJ			51.7	ps	9,10
Total Jitter Contribution < 4.25 Gb/s	RX Δ TJ			122.4	ps	10
Deterministic Jitter Contribution = 4.25 Gb/s	RX Δ DJ			25.9	ps	9,10
Total Jitter Contribution = 4.25 Gb/s	RX Δ TJ			61.2	ps	10

Notes:
1. Non-condensing.
2. Module power consumption never exceeds 1W.
3. AC coupled.
4. Or open circuit.
5. Into 100 ohm differential termination.
6. 20 – 80 %.
7. LOS is LVTTL. Logic 0 indicates normal operation; logic 1 indicates no signal detected.
8. All transceiver specifications are compliant with a power supply sinusoidal modulation of 20 Hz to 1.5 MHz up to specified value applied through the power supply filtering network shown on page 23 of the Small Form-factor Pluggable (SFP) Transceiver MultiSource Agreement (MSA)[6], September 14, 2000. The Power Supply Rejection applies for a supply voltage range of 3.1 to 3.6 V.
9. Measured with DJ-free data input signal. In actual application, output DJ will be the sum of input DJ and Δ DJ.
10. For 8.5 Gb/s operation, Deterministic Jitter and Total Jitter are not specified per FC-PI-4 Rev 8.00. Jitter values for gamma T and gamma R are controlled by TDP and stressed receiver sensitivity.

IV. Optical Characteristics (T_{OP} = -5 to 85 °C, V_{CC} = 3.00 to 3.60 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Transmitter						
Output Opt. Power, 8.5 Gb/s	$P_{O,RH}$	-8.4		+0.5	dBm	2
Output Opt. Power, 2.125, 4.25 Gb/s	$P_{O,RL}$	-8.4		-3	dBm	3
Optical Wavelength	λ	1285		1345	nm	4
Spectral Width	σ			1	nm	4
Optical Modulation Amplitude	OMA	290			μW	4,5
Transmitter and Dispersion Penalty, 8.5 Gb/s	TDP			3.2	dB	6
Optical Rise/Fall Time, 2.125, 4.25 Gb/s	t_r/ t_f			90	ps	7
RIN				-128	dB/Hz	
Receiver						
Unstressed Receiver OMA Sensitivity, 8.5 Gb/s	R_{SENSr}			0.042	mW	8
Unstressed Receiver OMA Sensitivity, 4.25 Gb/s	R_{SENS4}			0.029	mW	8
Unstressed Receiver OMA Sensitivity, 2.125 Gb/s	R_{SENS2}			0.015	mW	8
Average Received Power	Rx_{MAX}			+0.5	dBm	
Optical Center Wavelength	λ_C	1260		1360	nm	
Return Loss		12			dB	
LOS De-Assert	LOS_D			-19	dBm	
LOS Assert	LOS_A	-30			dBm	
LOS Hysteresis		0.5			dB	

Notes:
1. Class 1 Laser Safety per FDA/CDRH and EN (IEC) 60825 regulations.
2. High Bandwidth Mode. Class 1 Laser Safety per FDA/CDRH and EN (IEC) 60825 regulations.
3. Low Bandwidth Mode. Class 1 Laser Safety per FDA/CDRH and EN (IEC) 60825 regulations.
4. Also specified to meet curves in FC-PI-4 Rev 8.00[1] Figures 21, 22, and 23, which allow trade-off between wavelength, spectral width and OMA.
5. Equivalent extinction ratio specification for Fibre Channel. Allows smaller ER at higher average power.
6. For 8.5 Gb/s operation, Jitter values for gamma T and gamma R are controlled by TDP and stressed receiver sensitivity.
7. Unfiltered, 20-80%. Complies with IEEE 802.3 (Gig. E), FC 1x and 2x eye masks when filtered.
8. Measured with conformance signals defined in FC-PI-4 Rev. 8.00 specifications. Value in OMA. Measured with PRBS 2^7-1 at 10^{-12} BER.

V. General Specifications

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Data Rate	BR	2.125		8.5	Gb/sec	1
Bit Error Rate	BER			10^{-12}		2
Max. Supported Link Length on 9/125 μm SMF , 2.125, 4.25, 8.5 Gb/s	L_{MAX1}		10		km	3

Notes:
1. 2x/4x/8x Fibre Channel compliant.
2. Tested with a PRBS 2^7-1 test pattern.
3. Distances are based on FC-PI-4 Rev. 8.00[1] and IEEE 802.3 standards.

VI. Environmental Specifications

These Finisar 1310nm Extended Temperature SFP+ transceivers have an operating temperature range from -5°C to +85°C case temperature.

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Case Operating Temperature	T_{op}	-5		85	°C	
Storage Temperature	T_{sto}	-40		85	°C	

VII. Regulatory Compliance

Finisar transceivers are Class 1 Laser Products and comply with US FDA regulations. These products are certified by TÜV and CSA to meet the Class 1 eye safety requirements of EN (IEC) 60825 and the electrical safety requirements of EN (IEC) 60950. Copies of certificates are available at Finisar Corporation upon request.

VIII. Digital Diagnostic Functions

Finisar FTLF1428P3BNV SFP+ transceivers support the 2-wire serial communication protocol as defined in the SFP MSA[6]. It is very closely related to the E^{2}PROM defined in the GBIC standard, with the same electrical specifications.

The standard SFP serial ID provides access to identification information that describes the transceiver's capabilities, standard interfaces, manufacturer, and other information.

Additionally, Finisar SFP transceivers provide a unique enhanced digital diagnostic monitoring interface, which allows real-time access to device operating parameters such as transceiver temperature, laser bias current, transmitted optical power, received optical power and transceiver supply voltage. It also defines a sophisticated system of alarm and warning flags, which alerts end-users when particular operating parameters are outside of a factory set normal range.

The SFP MSA defines a 256-byte memory map in E^{2}PROM that is accessible over a 2-wire serial interface at the 8 bit address 1010000X (A0h). The digital diagnostic monitoring interface makes use of the 8 bit address 1010001X (A2h), so the originally defined serial ID memory map remains unchanged. The interface is identical to, and is thus fully backward compatible with both the GBIC Specification and the SFP Multi Source Agreement. The complete interface is described in Finisar Application Note AN-2030: "Digital Diagnostics Monitoring Interface for SFP Optical Transceivers".

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through a 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL, Mod Def 1) is generated by the host. The positive edge clocks data into the SFP transceiver into those segments of the E^{2}PROM that are not write-protected. The negative edge clocks data from the SFP transceiver. The serial data signal (SDA, Mod Def 2) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially.

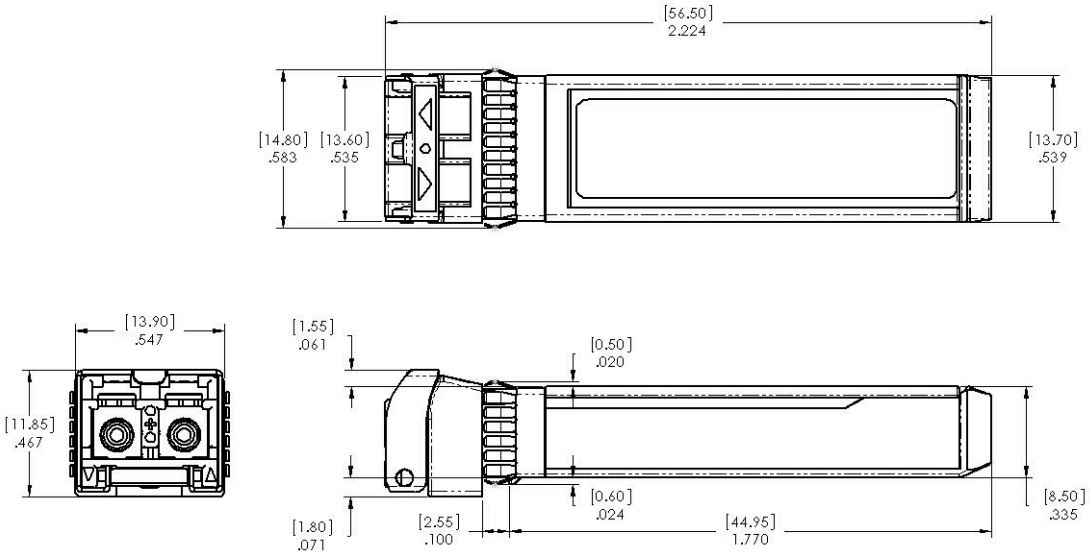
For more information, please see the SFP MSA documentation[3,6] or Finisar Application Note AN-2030.

FTLF1428P3BNV transceivers can be used in host systems that require either internally or externally calibrated digital diagnostics.

Please note that evaluation board FDB-1018 is available with Finisar ModDEMO software that allows simple to use communication over the 2-wire serial interface.

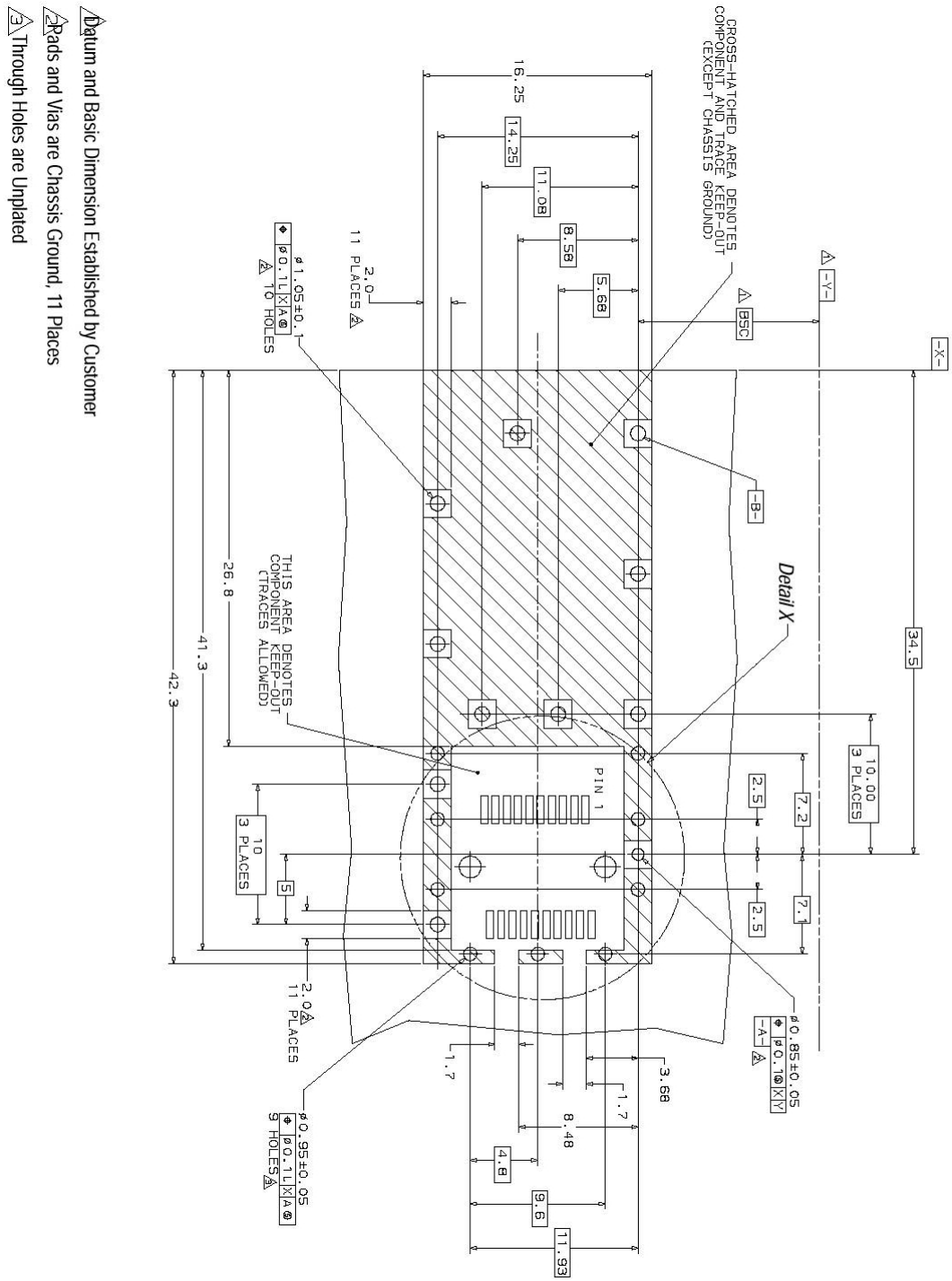
IX. Mechanical Specifications

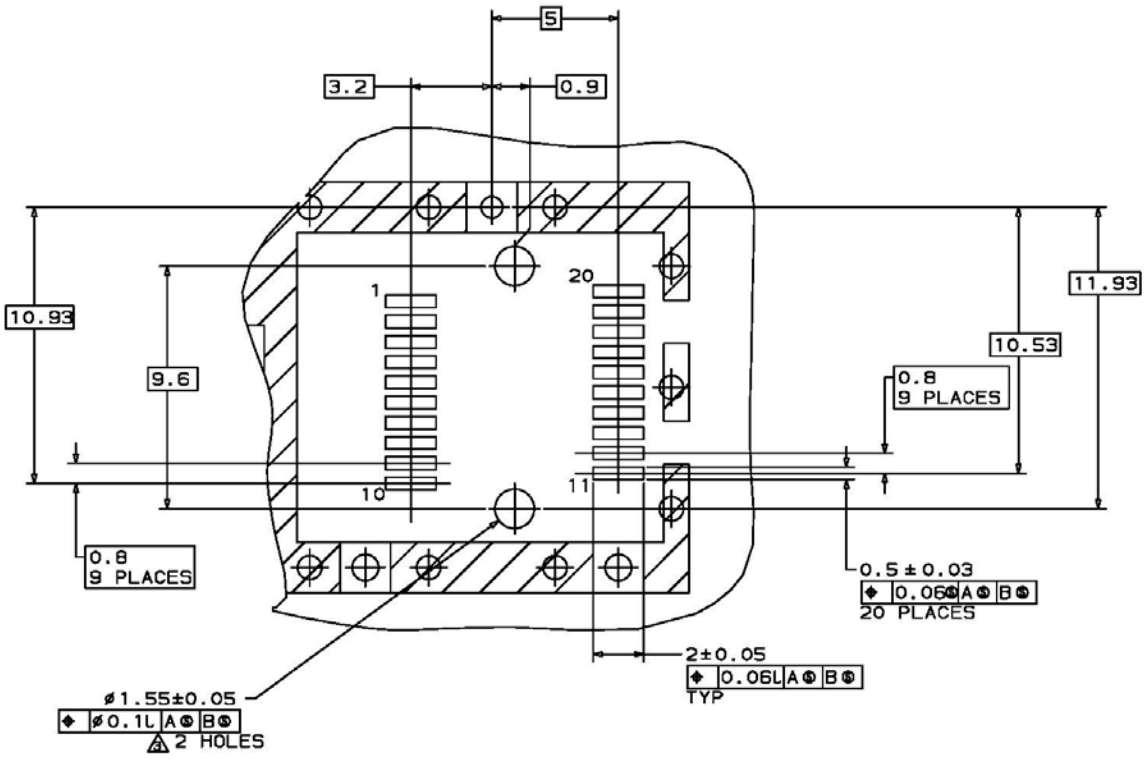
Finisar's FTLF1428P3BNV SFP+ transceivers are compatible with the SFF-8432[2] specification for improved pluggable form factor.

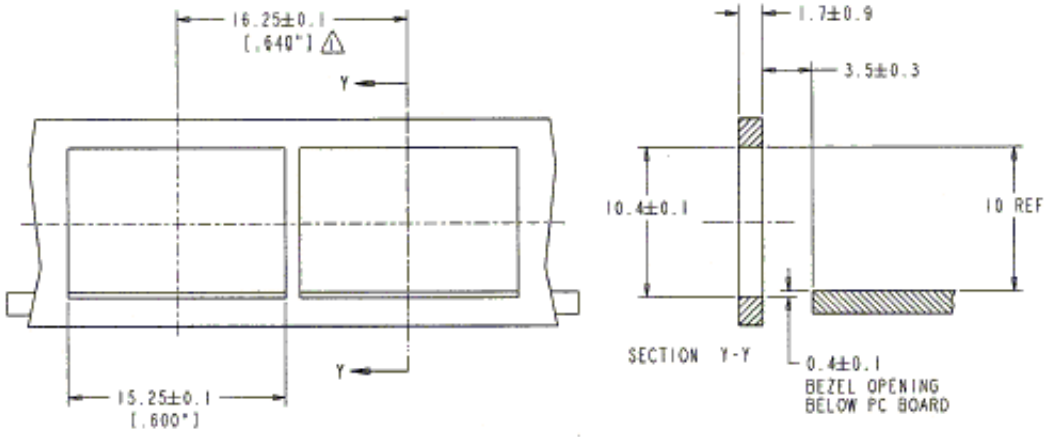


FTLF1428P3BNV

X. PCB Layout and Bezel Recommendations







NOTES:

1. MINIMUM PITCH ILLUSTRATED, ENGLISH DIMENSIONS ARE FOR REFERENCE ONLY
2. NOT RECOMMENDED FOR PCI EXPANSION CARD APPLICATIONS

XI. Timing Parameters for SFP+ Management (Table 7 of SFF-8431[4])

FTLF1428P3BNV transceiver module is fully compliant with the timing requirements of control and status I/O defined in the Table 7 of SFF-8431 (see below). Because FTLF1428P3BNV is a non-cooled power level 1 product, the parameter of "t_start_up_cooled", "t_power_level2", "t_power_down", "TX_Fault_on_cooled" defined in the Table 7 of SFF-8431 are not applicable.

Table 7 Timing Parameters for SFP+ Management

Parameter	*Symbol*	*Min.*	*Max.*	*Unit*	*Conditions*
TX_Disable assert time	t_off		100	µs	rising edge of TX_Disable to fall of output signal below 10% of nominal
TX_Disable negate time	t_on		2	ms	Falling edge of Tx_Disable to rise of output signal above 90% of nominal. This only applies in normal operation, not during start up or fault recovery.
Time to initialize 2-wire interface	t_2w_start_up		300	ms	From power on or hot plug after the supply meeting Table 8.
Time to initialize	t_start_up		300	ms	From power supplies meeting Table 8 or hot plug or Tx disable negated during power up, or Tx_Fault recovery, until non-cooled power level I part (or non-cooled power level II part already enabled at power level II for Tx_Fault recovery) is fully operational.
Time to initialize cooled module and time to power up a cooled module to Power Level II	t_start_up_cooled		90	s	From power supplies meeting Table 8 or hot plug, or Tx disable negated during power up or Tx_Fault recovery, until cooled power level I part (or cooled power level II part during fault recovery) is fully operational. Also, from falling edge of stop bit enabling Power Level II until cooled module is fully operational
Time to Power Up to Level II	t_power_level2		300	ms	From falling edge of stop bit enabling power level II until non-cooled module is fully operational
Time to Power Down from Level II	t_power_down		300	ms	From falling edge of stop bit disabling power level II until module is within power level I requirements
TX_Fault assert	TX_Fault_on		1	ms	From occurrence of fault to assertion of TX_Fault
TX_Fault assert for cooled module	TX_Fault_on_cooled		50	ms	From occurrence of fault to assertion of TX_Fault
TX_Fault Reset	t_reset	10		µs	Time TX_Disable must be held high to reset TX_Fault
RS0, RS1 rate select timing for FC	t_RS0_FC, t_RS1_FC		500	µs	From assertion till stable output
RS0, RS1 rate select timing non FC	t_RS0, t_RS1		10	ms	From assertion till stable output
Rx_LOS assert delay	t_los_on		100	µs	From occurrence of loss of signal to assertion of Rx_LOS
Rx_LOS negate delay	t_los_off		100	µs	From occurrence of presence of signal to negation of Rx_LOS

XII. SFP+ 2-wire Timing Specifications (Table 22 of SFF-8431[4])

FTLF1428P3BNV transceiver module is fully compliant with the SFP+ 2-wire timing specification defined in the Table 22 of SFF-8431 (see below).

Table 22 SFP+ 2-wire Timing Specifications

Parameter	*Symbol*	*Min.*	*Max.*	*Unit*	*Conditions*
Clock Frequency	f_{SCL}	0	400	kHz	Module shall operate with f_{SCL} up to 100 kHz without requiring clock stretching. The module may clock stretch with f_{SCL} greater than 100 kHz and up to 400 kHz.
Clock Pulse Width Low	t_{LOW}	1.3		µs	
Clock Pulse Width High	t_{HIGH}	0.6		µs	
Time bus free before new transmission can start	t_{BUF}	20		µs	Between STOP and START and between ACK and ReSTART
START Hold Time	$t_{HD,STA}$	0.6		µs	
START Set-up Time	$t_{SU,STA}$	0.6		µs	
Data In Hold Time	$t_{HD,DAT}$	0		µs	
Data In Set-up Time	$t_{SU,DAT}$	0.1		µs	
Input Rise Time (100 kHz)	$t_{R,100}$		1000	ns	From ($V_{IL,MAX}$ - 0.15) to ($V_{IH,MIN}$ + 0.15)
Input Rise Time (400 kHz)	$t_{R,400}$		300	ns	From ($V_{IL,MAX}$ - 0.15) to ($V_{IH,MIN}$ + 0.15)
Input Fall Time (100 kHz)	$t_{F,100}$		300	ns	From ($V_{IH,MIN}$ + 0.15) to ($V_{IL,MAX}$ - 0.15)
Input Fall Time (400 kHz)	$t_{F,400}$		300	ns	From ($V_{IH,MIN}$ + 0.15) to ($V_{IL,MAX}$ - 0.15)
STOP Set-up Time	$t_{SU,STO}$	0.6		µs	

XIII. SFP+ Memory Specifications (Table 23 of SFF-8431[4])

FTLF1428P3BNV transceiver module is fully compliant with the SFP+ memory specification defined in the Table 23 of SFF-8431 (see below).

Table 23 SFP+ Memory Specifications

Parameter	*Symbol*	*Min.*	*Max.*	*Unit*	*Conditions*
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold		500	µs	Maximum time the SFP+ module may hold the SCL line low before continuing with a read or write operation
Complete Single or Sequential Write up to 4 Byte	t_{WR}		40	ms	
Complete Sequential Write of 5-8 Byte	t_{WR}		80	ms	
Endurance (Write Cycles)		10 k		cycles	

XIV. References

1. "Fibre Channel Physical Interface-4 Specification (FC-PI-4 Rev. 8.00)". American National Standard for Information Technology, May 21, 2008.

2. "Improved Pluggable Formfactor", SFF Document Number SFF-8432, Revision 5.0, July 16, 2007.

3. "Digital Monitoring Interface for Optical Transceivers", SFF Document Number SFF-8472, Revision 10.3, December 1, 2007.

4. "Enhanced Specification for 8.5 and 10 Gigabit Small Form Factor Pluggable Module 'SFP+ '", SFF Document Number SFF-8431, Revision 3.0, May 8, 2008.

5. Directive 2011/65/EU of the European Council Parliament and of the Council, "on the restriction of the use of certain hazardous substances in electrical and electronic equipment". Certain products may use one or more exemptions as allowed by the Directive.

6. "Application Note AN-2038: Finisar Implementation of RoHS Compliant Transceivers".

7. Small Form Factor Pluggable (SFP) Transceiver Multi-source Agreement (MSA), September 14, 2000.

XV. For More Information

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