FTCE4516E1PCM

800G-DR8 QSFP-DD800 Optical Finisar® Transceiver

Finisar's FTCE4516E1PxM DR8 QSFPDD-800 transceiver modules are designed for use in 800 Gigabit Ethernet links on up to 500m of single mode fiber. They are compliant with the QSFPDD MSA, IEEE 802.3bs[3] and IEEE P802.3ck[7] Digital diagnostic functions are available via the I2C interface, as specified by the QSFP-DD MSA. The optical transceiver is RoHS compliant as described in Application Note AN-2038[4,5].

FEATURES

- Hot-pluggable QSFP-DD800 Type 2A form factor
- Supports 850Gb/s aggregate bit rate
- CMIS 5.0 (CMIS 4 optional)
- Case temperature range 0°C to +70°C (c-temp)
- Up to 500 Meter Parallel SMF
- Aligned with IEEE 802.3bs
- 8x100G PAM4 retimed 106.25Gb/s PAM4 electrical interface aligned to IEEE 802.3ck
- MPO-16
- I2C management interface
- Max Power 17W

APPLICATIONS

- 800G DR8 applications with FEC
- 2 x 400Gbe DR4
- 8 x 100GbE breakout applications

COHERENT

Product Selection

FTCE4516E1PCM

E: Ethernet protocol
P: Pull-tab type release
x: C = Commercial or L limited temperature range
y: M =MPO16,

I. Pin Descriptions

The electrical pinout of the QSFPDD-800 module is shown in Figure 1 below

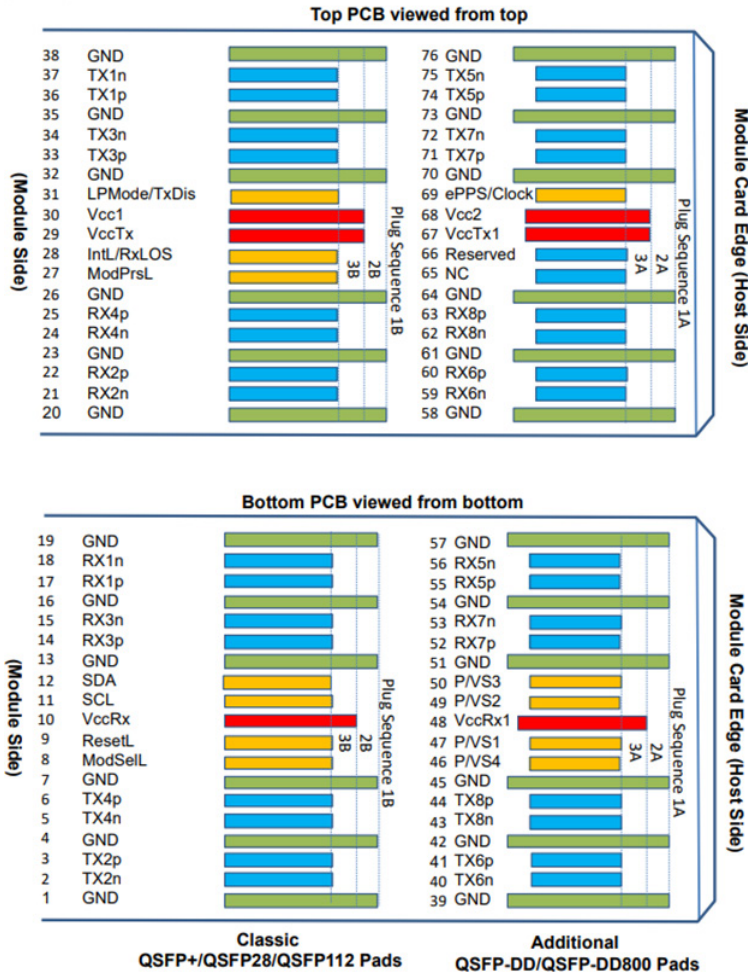

Figure 1 – QSFPDD-800 Module Pinout (per QSFPDD-800 MSA)

Pin	Logic	Symbol	Name/Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		Vcc Rx	+3.3 V Power supply receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL/ RxLOS	Interrupt	3B	
29		Vcc Tx	+3.3 V Power supply transmitter	2B	2
30		Vcc1	+3.3 V Power Supply	2B	2
31	LVTTL-I	LPMode/TxDis	Low Power mode/optional TX Disable	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1

43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46	LVCMOS/CML-I	P/VS4	Progra mmableJModule Vendor Specific 4	3A	5
47	LVCMOS/CML-I	VS1	Progra mmableJModule Vendor Specific 1	3A	5
48		VccRx1	3.3 V Power Supply	2A	2
49	LVCMOS/CML-O	P/VS2	Progra mmableJModule Vendor Specific 2	3A	5
50	LVCMOS/CML-O	P/VS3	Progra mmableJModule Vendor Specific 3	3A	5
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Input	3A	
53	CML-O	Rx7n	Receiver Inverted Data Input	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Input	3A	
56	CML-O	Rx5n	Receiver Inverted Data Input	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Non-Inverted Data Input	3A	
60	CML-O	Rx6p	Receiver Inverted Data Input	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Non-Inverted Data Input	3A	
63	CML-O	Rx8p	Receiver Inverted Data Input	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For Future Use	3A	3
67		VccTx1	3.3 V Power Supply	2A	2
68		Vcc2	3.3 V Power Supply	2A	2
69	LVCMOS-I	ePPS/Clock	1PPS PTP clock or reference clock input	3A	6
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	TransmitterInverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Notes
Note 1: QSFP-DD uues common ground (GND) for all singnals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board sgnal-common ground plane.
Note 2: VccRx, VccRx1, Vcc;, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 4. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins and each rated for a maximum current of 1000 mA.
Note 3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.
Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence specifies the mating sequence of the host connector and module, The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B followed by 3A, 3B.
Note 5: Full definit ions of !he PNSx signa'ls ourrenlly under development On new designs mot used PN Sx signals are recommended to, be terminaled om the host with 10 kΩ.
Note 6: ePPS/Clock 1if not used reoommend'ed to be terminated with 50 Ω to ,ground ,on lhe host

II. Absolute Maximum Ratings

Module performance is not guaranteed beyond the operating range (see Section VI). Exceeding the limits below may damage the transceiver module permanently.

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Maximum Supply Voltage	Vcc	-0.5		4.0	V	
Storage Temperature	T_S	-40		+85	℃	
Case Operating Temperature	T_{OP}	0 tbd		+70 tbd	℃	C-temp L-temp
Relative Humidity	RH	15		85	%	1
Receiver Damage Threshold, per Lane	P_{Rdmg}	5			dBm	

Notes:
1. Non-condensing.

III. Electrical Characteristics (EOL, TOP = 0 to 70 ℃, V_{cc} = 3.135 to 3.465 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Supply Current	Icc			tbd	A	
Module total power	P			17.5	W	1
Transmitter						
Signaling rate per lane		53.125± 100 ppm.			Gbd	
Differential data input voltage per lane		900			mV	
Differential to common mode input re-turn loss		Per equation (83E–6) IEEE802.3bm			dB	
Effective return loss, ERL		8.5			dB	
Differential termination mismatch				10	%	
Module stress input test		Per 120E.3.4.1 IEEE802.3bs				2
Single-ended voltage tolerance range		-0.4		3.3	V	
DC common mode voltage		-350		2850	mV	3
Receiver						
Signaling rate per lane		53.125			Gbd	
AC common-mode output voltage (RMS)				17.5	mV	
Differential output voltage				900	mV	
Eye height, differential		15			mV	
Vertical eye closure				12	dB	
Common-mode to differential return loss		Equation (120G-1)			dB	
Effective return loss, ERL		8.5			dB	
Differential termination mismatch				10	%	
Transition time (min, 20% to 80%)		8.5			ps	
DC common mode voltage		-350		2850	mV	3,4

Notes:
1. Maximum total power value is specified across the full temperature and voltage range.
2. Meets BER specified in 120G.1.1.
3. DC common-mode voltage is generated by the host. Specification includes effects of ground offset voltage
4. The signaling rate range is derived from the PMD receiver input.

IV. Optical Characteristics (EOL, T_{OP} = 0 to 70 °C, V_{CC} = 3.135 to 3.465 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Transmitter						
Signaling rate (each lane (range)		53.125 ± 100 ppm			GBd	
Modulation format		PAM4				
Lane wavelength (range)		1304.5 to 1317.5			nm	
Side-mode suppression ratio (SMSR)		30			dB	
Average launch power, each lane				4.5	dBm	
Average launch power, each lane		-2			dBm	1
Outer Optical Modulation Amplitude (OMAouter), each lane		-0.8		4.2	dBm	2
Launch power in OMAouter minus TDECQ, each lane		-2.2			dBm	
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane				3.4	dB	
Average launch power of OFF transmitter, each lane				-15	dBm	
Extinction ratio		3.5			dB	
$RIN_{21.4}$ OMA				-136	dB/Hz	
Optical return loss tolerance				21.4	dB	
Transmitter reflectance				-26	dB	3

Notes:
1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Even if the TDECQ < 1.4 dB, the OMAouter (min) must exceed this value
3. Transmitter reflectance is defined looking into the transmitter

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Receiver						
Signaling rate (each lane (range)			53.125 ± 100 ppm		GBd	
Modulation format			PAM4			
Lane wavelength (range)			1304.5 to 1317.5		nm	
Damage threshold, each lane			5		dBm	1
Average receive power, each lane				4	dBm	
Average receive power, each lane		-5.9			dBm	2
Receive power (OMAouter), each lane				4.2	dBm	
Receiver reflectance				-26	dB	
Receiver sensitivity (OMAouter), each lane				-4.4	dBm	3
Stressed receiver sensitivity (OMAouter), each lane				-1.9	dBm	4
Conditions of stressed receiver sensitivity test:						
Stressed eye closure for PAM4 (SECQ)			3.4		dB	5
OMAouter of each aggressor lane			4.2		dBm	6

Notes:
1. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
2. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
3. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with SECQ of 0.9 dB.
4. Measured with conformance test signal at TP3 (see 124.8.9) for the BER specified in 124.1.1.
5. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

V. General Specifications

Parameter	Value	Units	Notes
Module Form Factor	QSFP-DD800 Type 2A		As defined by QSFP-DD
Number of Lanes	8 Tx and 8 Rx		
Maximum Aggregate Data Rate	850	Gb/s	Note 1.
Maximum Data Rate per Lane	53.125± 100 ppm.	GBd	
Link Distance	500	meters	2km version available
Protocols supported	400G/800G Ethernet		
Electrical Interface and Pin-out	76-pin edge connector		Pin-out as defined by QSFP-DD
Standard Optical Cable Type	SMF G.652		
Maximum Power Consumption per End	17.5W (retimed Tx)	Watts	Maximum total power value is specified across the full temperature and voltage range
Management Interface	Serial, I2C-based, 1 MHz maximum frequency		As defined in CMIS 5.1

Data Rate Specifications	Symbol	Min	Typ	Max	Units	Ref/
Bit Rate per Lane	BR	53.125± 100 ppm.			GBd	
Pre-FEC Bit Error Ratio	BER			$2.4e^{-4}$		2

Notes:
1. Supports 400GBASE-DR4 per IEEE P802.3bs.
2. As defined by IEEE P802.3bs.

VI. Environmental Specifications

Finisar FTCE4516E1PCM DR8 QSFPDD-800 transceivers have an operating case temperature range of 0°C to +70°C.

Environmental Specifications	Symbol	Min	Typ	Max	Units	Ref.
Case Operating Temperature	T_{op}	0		70	°C	
Storage Temperature	T_{sto}	-40		85	°C	

VII. Regulatory Compliance

The FTCE4516E1PCM transceivers are RoHS compliant. Copies of certificates are available from Coherent Corp. upon request.

The FTCE4516E1PCM transceiver modules are Class 1 laser eye safety compliant per IEC 60825-1.

CAUTION: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

VIII. Digital Diagnostics Functions

FTCE4516E1PxM DR8 QSFPDD-800 transceivers support the I2C-based diagnostics interface specified by the SFF Commitee1.

IX. Management Interface

Modules shall be compliant to Common Management Interface Specification (CMIS) Rev. 5.0. Other CMIS versions upon customer request.

The following AppSel are supported: 8x100 Application1
2x400 Application2 4x200 Application3

Firmware Upgrade through CDB is supported PRBS generation and checking is supported

X. Mechanical Specifications

Finisar FTCE4516E1PxM DR8 QSFPDD-800 transceivers are compatible with the QSFPDD-800 Specification for pluggable form factor modules.

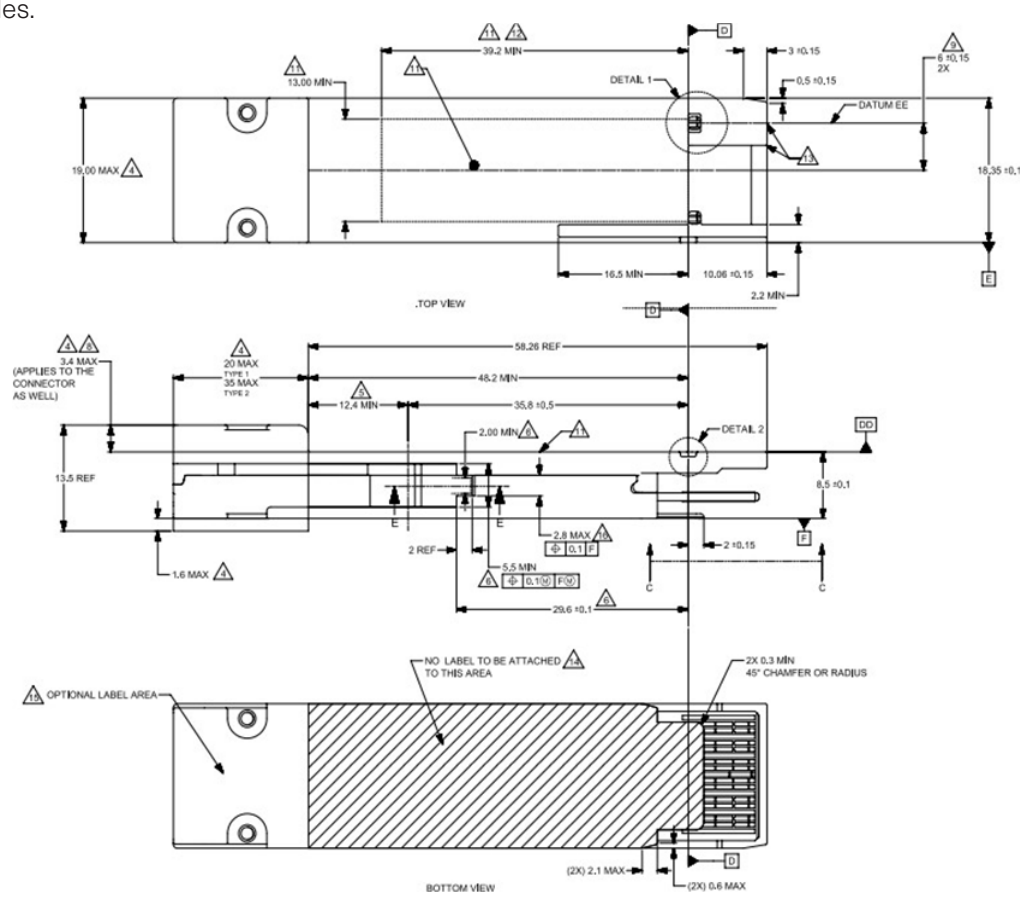

Figure 2. FTCE4516E1PxM Mechanical Dimensions.

Figure 3. Product Label

XII. References

1. QSFP-DD/QSFP-DD800/QSFP112 Hardware Specification Rev 6.01

2. SFF-8665: “QSFP+ 28Gb/s 4X Pluggable Transceiver Solution (QSFP28)”, Rev 1.9, June 29, 2015 and associated SFF documents referenced therein:
i. SFF-8661
ii. SFF-8679
iii. SFF-8662
iv. SFF-8663
v. SFF-8672

3. IEEE P802.3bs, 400GBASE-DR4

4. Directive 2011/65/EU of the European Council Parliament and of the Council, “on the restriction of the use of certain hazardous substances in electrical and electronic equipment” as well as Commission Delegated Directive (EU) 2015/863 amending Annex II to Directive 2011/65/EU. Certain products may use one or more exemptions as allowed by the Directive.

5. Application Note AN-2038: “II-VI Implementation of RoHS Compliant Transceivers”.

6. Common Management Interface Specification (CMIS) Rev 5.1, 5.0 and 4.0.
7. IEEE P802.3ckTM/D3.0 Physical Layer Specifications and Management Parameters for 100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical Interfaces Based on 100 Gb/s Signaling, 400GAUI-4 C2M

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