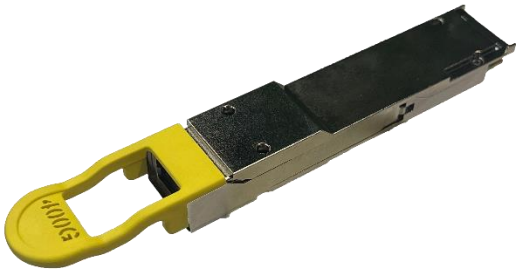
Product Specification

400GBASE-DR4+ QSFP112 Optical Transceiver Module

FTCD4538E1PCM

PRODUCT FEATURES

- Hot-pluggable QSFP112 form factor type 2
- Supports 425Gb/s aggregate bit rate
- Power dissipation <8.5W
- RoHS-6 compliant
- Case temperature range 0°C to +70°C (c-temp)
- Single 3.3V power supply
- Aligned with IEEE 802.3bs
- 4x100Gb/s PAM4 serial lanes
- 4x100G PAM4 retimed electrical interface
- Parallel MPO 12 receptacle
- I2C management interface



APPLICATIONS

- 400G DR4+ applications with FEC
- 100GbE breakout applications

Finisar's FTCD4538E1PCM DR4+ QSFP112 transceiver modules are designed for use in 400 Gigabit Ethernet links on up to 2km of single-mode fiber. They are compliant with the QSFP112 MSA, and portions of IEEE P802.3. Digital diagnostic functions are available via the I2C interface, as specified by the QSFP 56 MSA and Finisar Application Note AN-20xx[5]. The transceiver is RoHS-6 compliant per Directive 2011/65/EU4 and Finisar Application Note AN-2038[5].

PRODUCT SELECTION

FTCD4538E1PCM (Application select 1 set to 4x100G mode)
FTCD4538E1PCM-4A (Application select 1 set to 400G mode)

E:	Ethernet protocol
P:	Pull-tab type release
C:	Commercial temperature range
M:	MPO receptacle

I. Pin Descriptions

Electrical Connector: The QSFP112 connector is a 38-contact connector. QSFP112 module contacts mate with the host in the order of ground, power, followed by a signal as illustrated by Figures and 2 and the contact sequence order listed in table 1

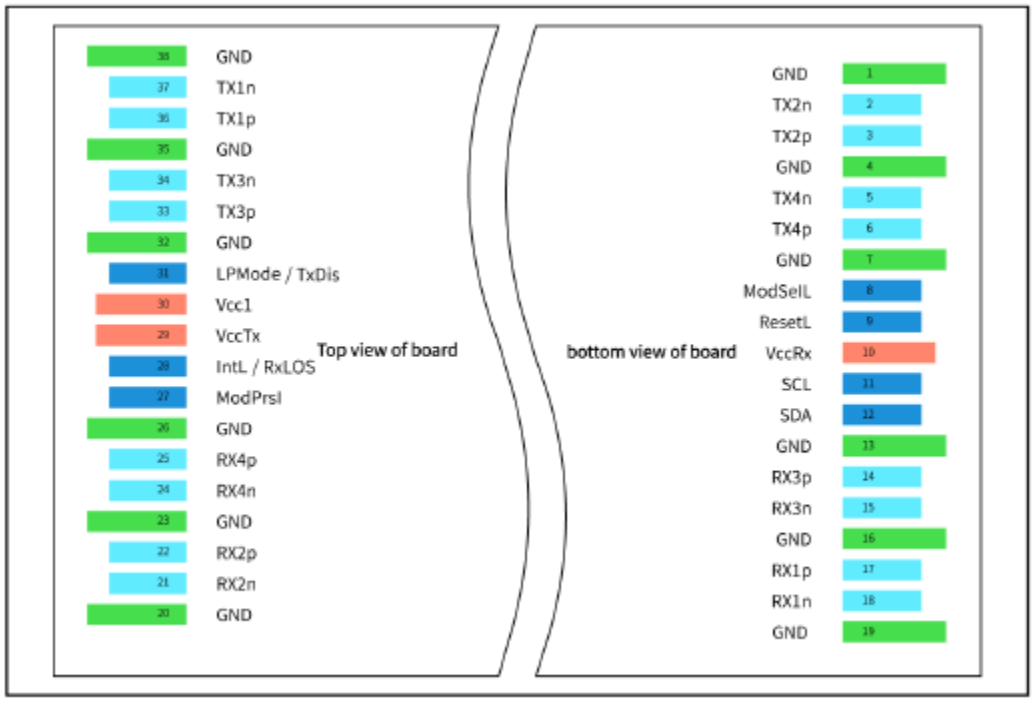


Figure 1 QSFP112 Module contact assignment

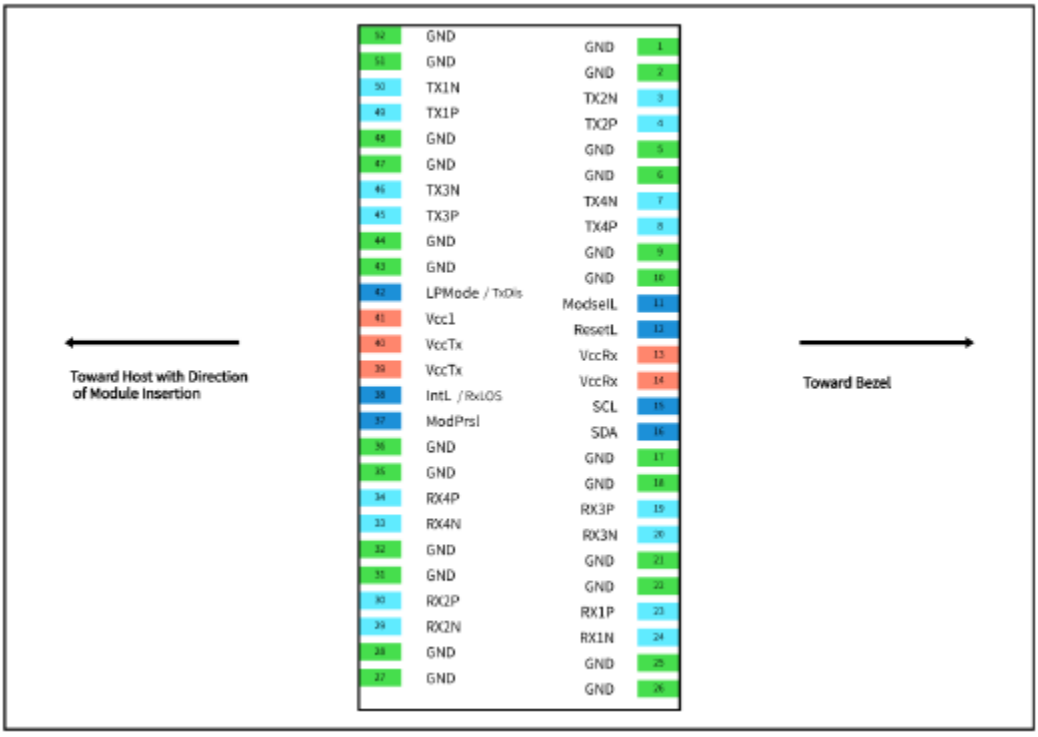


Figure 2 QSFP112 Host PCB pad assignment

Table 1 QSFP112 Module contact and Host PCB pad electrical definition

Host PCB pad	Module contact	Logic	Symbol	Description	Plug Sequence	Notes
1	1		GND	Ground	1	1
2			GND	Ground	1	1
3	2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
4	3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
5	4		GND	Ground	1	1
6			GND	Ground	1	1
7	5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
8	6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
9	7		GND	Ground	1	1
10			GND	Ground	1	1
11	8	LVTTL-I	ModSelL	Select	3	
12	9	LVTTL-I	ResetL	Reset	3	
13	10		Vcc Rx	+3.3 V Power supply receiver	2	2
14			Vcc Rx	+3.3 V Power supply receiver	2	2
15	11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
16	12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
17	13		GND	Ground	1	1
18			GND	Ground	1	1
19	14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
20	15	CML-O	Rx3n	Receiver Inverted Data Output	3	
21	16		GND	Ground	1	1
22			GND	Ground	1	1
23	17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
24	18	CML-O	Rx1n	Receiver Inverted Data Output	3	
25	19		GND	Ground	1	1
26			GND	Ground	1	1
27	20		GND	Ground	1	1
28			GND	Ground	1	1
29	21	CML-O	Rx2n	Receiver Inverted Data Output	3	
30	22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
31	23		GND	Ground	1	1
32			GND	Ground	1	1
33	24	CML-O	Rx4n	Receiver Inverted Data Output	3	
34	25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
35	26		GND	Ground	1	1
36			GND	Ground	1	1
37	27	LVTTL-O	ModPrsL	Present	3	
38	28	LVTTL-O	IntL/RxLOS	Interrupt/optional RxLOS	3	
39	29		Vcc Tx	+3.3 V Power supply transmitter	2	2
40			Vcc Tx	+3.3 V Power supply transmitter	2	2
41	30		Vcc1	+3.3 V Power Supply	2	2
42	31	LVTTL-I	LPMode/TxDis	Low Power Mode/optional TX Disable	3	
43	32		GND	Ground	1	1
44			GND	Ground	1	1
45	33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
46	34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
47	35		GND	Ground	1	1
48			GND	Ground	1	1
49	36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
50	37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
51	38		GND	Ground	1	1
52			GND	Ground	1	1

Note 1: GND is the symbol for signal and supply (power) common for the QSFP112 module. All are common within the QSFP112 module and all voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements, defined for the host side of the Host Edge Card Connector, are listed in Table 4. Recommended host board power supply filtering is shown in Figure 4. Vcc Rx, Vcc1and Vcc Tx may be internally connected within the QSFP112 module in any combination. The connector pins are each rated for a maximum current of 1.5A (max. current of 2.0 A is required for high module power of 15-20W).

II. Absolute Maximum Ratings

Module performance is not guaranteed beyond the operating range (see Section VI). Exceeding the limits below may damage the transceiver module permanently.

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Maximum Supply Voltage	Vcc	-0.5		3.6	V	
Storage Temperature	T_S	-40		+85	°C	
Case Operating Temperature	T_{OP}	0		+70	°C	c-temp
Relative Humidity	RH	15		85	%	8
Receiver Damage Threshold, per Lane	P_{Rdmg}	5			dBm	
Power Supply Noise including ripple				50	mV	
Module Maximum Current Inrush with LPMode Pin deasserted				0.55	A	
Module Current Ramp Rate				100	mA/µS	

Notes:
1. Non-condensing.

III. Electrical Characteristics (EOL, T_{OP} = 0 to +70 °C, V_{CC} = 3.135 to 3.465 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Supply Current	Icc			2.77	A	
Module total power	P			8.5	W	8
Transmitter						
Signaling rate per lane		53.125± 50 ppm.			Gbd	
Differential data input voltage per lane	Vin,pp,diff	750			mV	5
Effective return loss, ERL (min)		7.3			dB	
Differential to common mode input return loss		Per equation (120-G1) IEEE802.3ck			dB	5
Differential termination mismatch				10	%	5
Module stress input test		Per 120G.3.4.3.1 IEEE802.3ck				5
Single-ended voltage tolerance range		-0.4		3.3	V	5
DC common mode voltage		-0.3		2.8	V	5
Steady-state voltage, vf(max)				375	mV	5
Receiver						
Signaling rate per lane		53.125± 50 ppm.			Gbd	
AC common-mode output voltage (RMS)				80	mV	5
Differential pk-pk voltage toterance (min)		750			mV	
Effective return loss, ERL (min)		8.5			dB	
Near-end Eye height, differential (min)		10			mV	
Module stress input tolerance		See 120G 3.4.3				5
Differential-mode to common-mode return loss		Per equation 120-G2 IEEE802.3ck			dB	5
Differential termination mismatch				10	%	
DC common mode voltage (min)		-0.3		2.8	V	5

Notes:
1. Maximum total power value is specified across the full temperature and voltage range.
2. Meets specified BER
3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

IV. Optical Characteristics (EOL, T_{OP} = 0 to +70 °C, V_{CC} = 3.135 to 3.465 Volts)

Meets 400GBASE-DR4 as being defined by IEEE P802.3bs

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Transmitter						
Signaling rate (each lane (range)		53.125 ± 100 ppm			GBd	
Modulation format		PAM4				
Lane wavelength (range)		1304.5 to 1317.5			nm	
Side-mode suppression ratio (SMSR)		30			dB	
Average launch power, each lane				4	dBm	
Average launch power, each lane		-2.4			dBm	8
Outer Optical Modulation Amplitude (OMAouter), each lane		-0.2		4.2	dBm	9
Launch power in OMAouter minus TDECQ, each lane		-1.6			dBm	
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane				3.4	dB	
Average launch power of OFF transmitter, each lane				-15	dBm	
Extinction ratio		3.5			dB	
$RIN_{21.4}OMA$				-136	dB/Hz	
Optical return loss tolerance				17.1	dB	
Transmitter reflectance				-26	dB	

Notes:
1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Even if the TDECQ < 1.4 dB, the OMAouter (min) must exceed this value
3. Transmitter reflectance is defined as looking into the transmitter

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Receiver						
Signaling rate (each lane (range)		53.125 ± 100 ppm			GBd	
Modulation format		PAM4				
Lane wavelength (range)		1304.5 to 1317.5			nm	
Damage threshold, each lane		5.5			dBm	1
Average receive power, each lane				4.5	dBm	
Average receive power, each lane		-6.4			dBm	2
Receive power (OMAouter), each lane				4.2	dBm	
Receiver reflectance				-26	dB	
Receiver sensitivity (OMAouter), each lane				-4.4	dBm	3
Stressed receiver sensitivity (OMAouter), each lane				-2.5	dBm	4
Conditions of stressed receiver sensitivity test:						
Stressed eye closure for PAM4 (SECQ), lane under test		3.4			dB	5
OMAouter of each aggressor lane		4.2			dBm	

Notes:

1. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
2. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
3. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with SECQ up to 3.4dB
4. Measured with conformance test signal at TP3 (see 124.8.9) for the BER specified in 124.1.1.
5. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

V. General Specifications

Parameter		Symbol	Min	Typ	Max	Units	Ref.
Bit Rate (all wavelengths combined)		BR			425	Gb/s	8
Bit Error Ratio		BER			2.4E-4		9
Maximum Supported Distances							
Fiber Type							
SMF per G.652		Lmax1			2	Km	

Notes:
1. Supports 400GBASE-DR4 per IEEE P802.3bs.
2. As defined by IEEE P802.3bs.

VI. Environmental Specifications

Finisar FTCD4538E1PCM DR4+ QSFP112 transceivers have an operating case temperature range of 0°C to +70°C.

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Case Operating Temperature	T_{op}	0		+70	°C	
Storage Temperature	T_{sto}	-40		+85	°C	

VII. Regulatory Compliance

Finisar FTCD4538E1PCM DR4+ QSFP112 transceivers are Class 1 Laser Products. They are certified per the following standards:

Feature	Agency	Standard
Laser Eye Safety	FDA/CDRH	CDRH 21 CFR 1040 and Laser Notice 56
Laser Eye Safety	UL/CSA/TÜV	IEC 60825-1:2014 IEC 60825-2: 2004+A1+A2
Electrical Safety	UL/CSA/TÜV	IEC 62368-1:2018

Copies of the referenced certificates are available at Finisar Corporation upon request.

CAUTION: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

VIII. Digital Diagnostics Functions

FTCD4538E1PCM DR4+ QSFP112 transceivers support the I2C-based diagnostics interface specified by the SFF Commitee[1]. See also Finisar Application Note AN-20xx (TBD).

IX. Memory Contents

Per QSFP112 MSA Specification[1]. See Finisar Application Note AN-20xx (TBD).

X. Mechanical Specifications

Finisar FTCD4538E1PCM DR4+ QSFP112 form factor mechanical dimensions

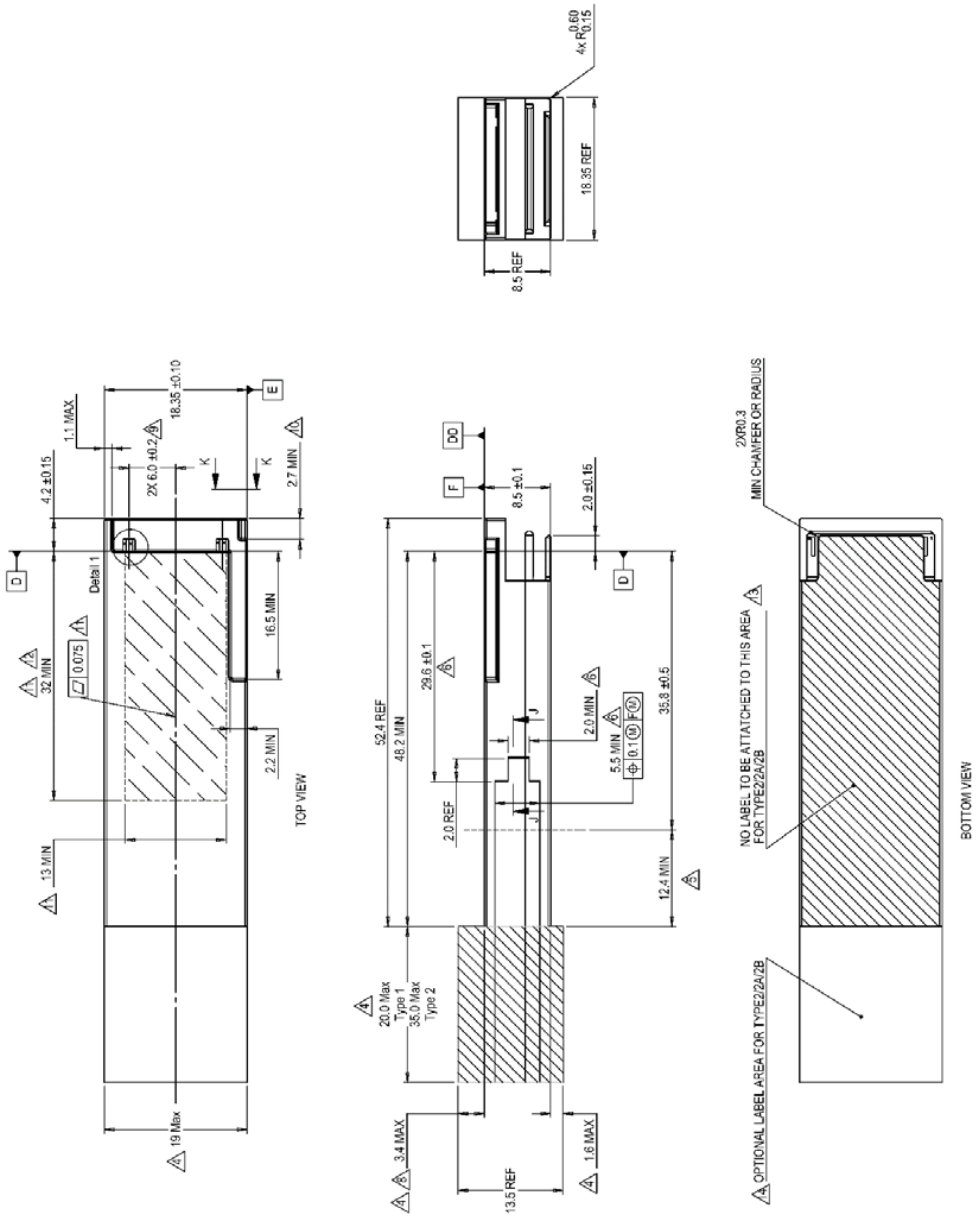


Figure 3.1 FTCD4538E1PCM Mechanical Dimensions Part 1

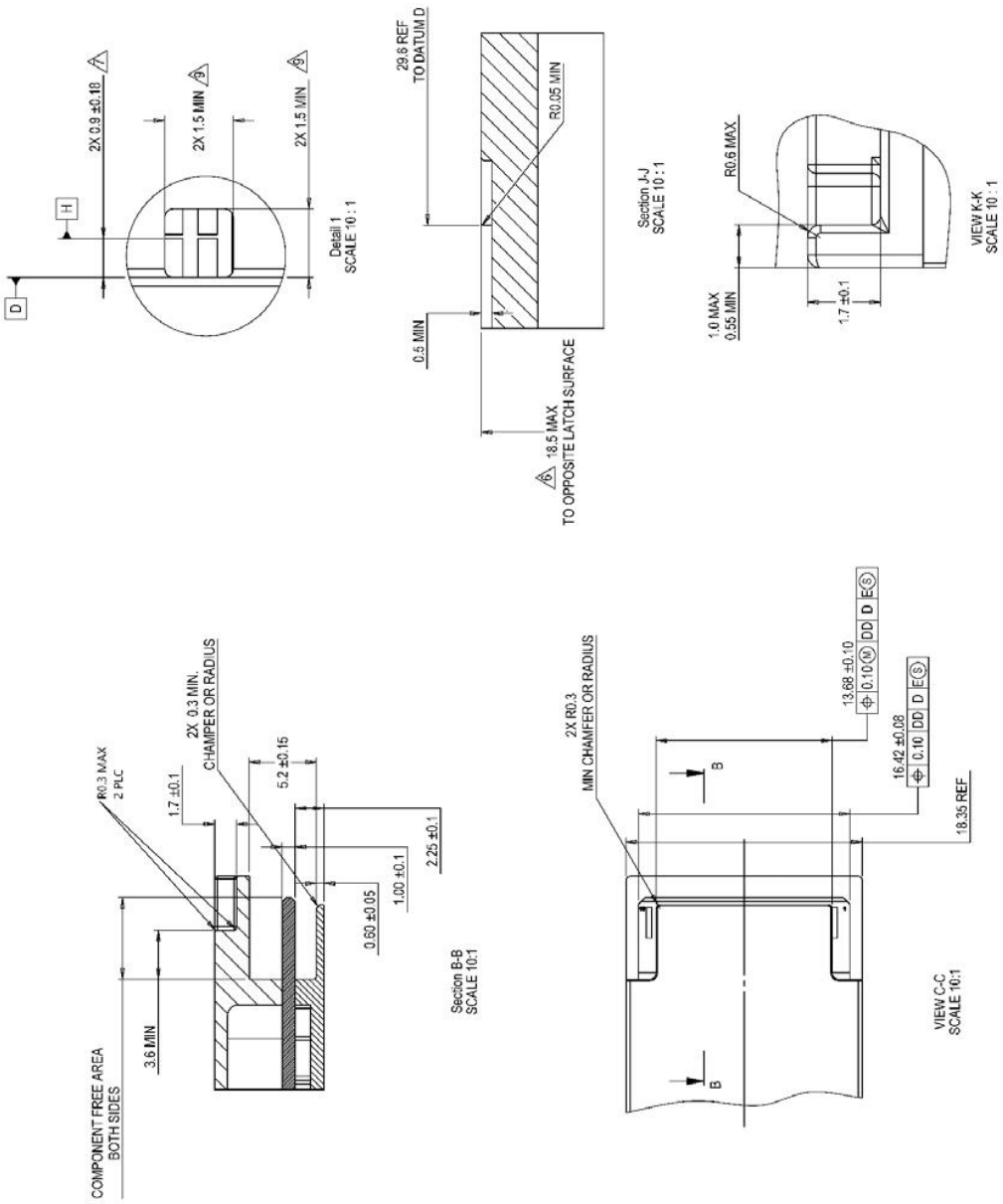


Figure 3.2 FTCD4538E1PCM Mechanical Dimensions Part 2

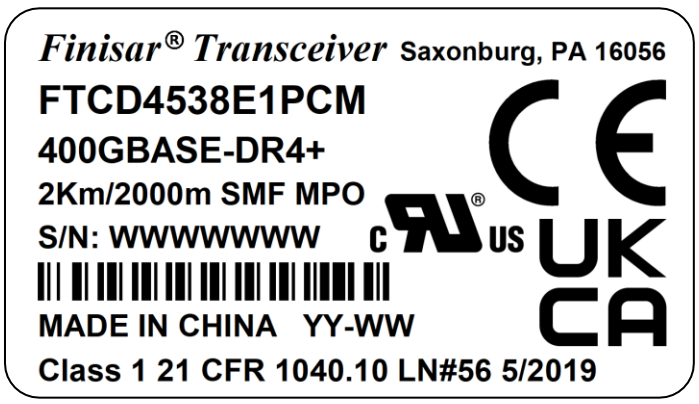


Figure 4. Product Label

XI. References

1. QSFP112_MSA_Specification_Rev2.0
2. QSFP-DD-Hardware-Rev6.01
3. OIF-CEI-56G-VSR-PAM4
4. OIF-CEI-112G-VSR-PAM4
5. IEEE 802.3ck Annex 120G(400GAUI-4 C2M)
6. IEEE 802.3bs(400GBASE-DR4)
7. 100G-FR and 100G-LR Technical Specifications Rev 2.0 (DR4+)
8. QSFP-DD Specification for QSFP Double Density 8X Pluggable Transceiver
9. 400G-LR4-10 Technical Spec rev1.0(LR4)
    - SFF-8024 Rev.4.6
    - SFF-8636 Rev.2.10a
    - SFF-8679 Rev.1.8
    - SFF-8665 Rev.1.9
10. Directive 2011/65/EU of the European Parliament and of the Council, "on the restriction of the use of certain hazardous substances in electrical and electronic equipment," July 1, 2011.
11. "Application Note AN-2038: Finisar Implementation Of RoHS Compliant Transceivers", Finisar Corporation, January 21, 2005.
12. Application Note AN-2153, Initialization, Finisar Corporation.
13. Application Note AN-2154, EEPROM Map, Finisar Corporation.
14. Application Note AN-2189, EEPROM Application, Coherent.

XII. For More Information:

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